



# AVED MEMORY PRODUCTS

Where Quality & Memory Merge

## AMP377P0823BT2-C75/H

8M X 72 SDRAM DIMM with PLL and Register, based on 8M X 8, 4 Banks, 4K Refresh, 3.3V Synchronous DRAMs WITH SPD

### DESCRIPTION

AVED Memory Products AMP377P0823BT2-C75/H is a 8M bit X 72 Synchronous Dynamic RAM high density memory module. The AVED Memory Products AMP377P0823BT2-C75/H consists of nine CMOS 8M X 8 bit Synchronous DRAMs in TSOP-II 400mil packages, two 18-bits Drive ICs for input control signal, one PLL in 24-pin TSSOP package for clock and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect on a 168-pin glass-epoxy substrate. Two 0.22uF and one 0.0022uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The AVED Memory Products AMP377P0823BT2-C75/H is a Dual In-Line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

### APPLICATION

Main Memory unit for computer, Microcomputer memory, Refresh memory for CRT.

### PIN NAMES

### FEATURES

#### • Performance Ranges

- Part Identification
  - AMP377P0823BT2-C75/H
  - 4096 cycles/64ms Ref, TSOP, Gold Contact Plating
  - PC133 Compliant

Part #	Maximum Frequency/Speed
AMP377P0823BT2-C75/H	133MHz (7.5ns @CL=3)

- Burst Mode Operation
- Auto & Self Refresh capability (4096 cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst Length (1, 2, 4, 8 & Full Page)
  - Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM

Pin Name	Function
A0 - A11	Address Input (multiplexed)
BA0 - BA1	Select Bank
DQ0 - DQ63	Data Input/Output
CB0 - 7	Check bit (Data-in/out)
CLK0	Clock Input
CKE0	Clock Enable Input
CS0, CS2	Chip Select Input
RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Write Enable
DQM0 - 7	DQM
VDD	Power Supply(3.3V)
Vss	Ground
*VREF	Power Supply for Reference
REGE	Register Enable
SDA	Serial Address Data I/O
SCL	Serial Clock
SA0 - 2	Address in EEPROM
WP	Write Protect
DU	Don't Use
NC	No connection



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### PIN CONFIGURATIONS (FRONT SIDE / BACK SIDE)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	* $\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	* $\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

Pins marked \* are not used in this module.

Pins marked \*\* should be NC in the system which does not support SPD.



**8M X 72 SDRAM DIMM with PLL and Register, based on 8M X 8, 4 Banks, 4K Refresh, 3.3V Synchronous DRAMs WITH SPD**

**PIN CONFIGURATION DESCRIPTION**

Pin	Name	Input Function
CLK	System Clock	Active on the positive going edge to sample all inputs.
$\overline{CS}$	Chip Select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE, and DQM.
CKE	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+ $t_{ss}$ prior to valid command.
A0 - A11	Address	Row/Column addresses are multiplexed on the same pins. Row Address: RA0 – RA11, Column address: CA0 – CA8
BA0 - BA1	Bank Select Address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	Row Address Strobe	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	Column Address Strobe	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	Write Enable	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$ , $\overline{WE}$ active.
DQM0 - DQM7	Data Input/Output Mask	Makes data output Hi-Z, $t_{SHZ}$ after the clock and masks the output. Blocks data input when DQM active. (Byte Masking)
REGE	Register Enable	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. The inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to VDD through 10K ohm Resistor on PCB. Therefore, if REGE of module is floating, this module will be operated as registered mode.
DQ0 - DQ63	Data Input/Output	Data inputs/outputs are multiplexed on the same pins.
CB0 - 7	Check bit	Check bits for ECC.
WP	Write Protect	WP pin is connected to Vss through 47K $\Omega$ Resistor. When WP is "high" EEPROM programming will be inhibited, and the entire memory will be write-protected.
VDD/Vss	Power Supply/Ground	Power and ground for the input buffers and the core logic.



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### ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	VIN, VOUT	-1.0 - 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 - 4.6	V
Storage Temperature	Tstg	-55 to + 150	°C
Power Dissipation	Pd	9	W
Short Circuit Current	IOS	50	mA

**Note:** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to higher than recommended voltage for extended periods may affect device reliability.

### DC OPERATING CONDITIONS AND CHARACTERISTICS Recommended operating conditions

(Voltage referenced to Vss=0V, Ta = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	VDD	3.0	3.3	3.6	V	-
Input logic high voltage	VIH	2.0	3.0	VDDQ+0.3	V	1
Input logic low voltage	VIL	-0.3	0	0.8	V	2
Output logic high voltage	VOH	2.4	-	-	V	IOH = -2mA
Output logic low voltage	VOL	-	-	0.4	V	IOL = 2mA
Input leakage current (Inputs)	ILI	-10	-	10	µA	3

**Note:**1. VIH(max) = 5.6V AC. Pulse width ≤ 3ns.

$\overline{\text{RAS}}$

2. VIL(min) = -2.0V AC. Pulse width ≤ 3ns

3. Any input 0V ≤ VIN ≤ VDDQ. Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

### CAPACITANCE (VDD = 3.3V, Ta = 23°C, f=1MHz, VREF = 1.4V ± 200mV)

Item	Symbol	Min	Max	Unit
Input capacitance [A0 - A11, BA0 - BA1]	CADD	-	15	pF
Input capacitance [ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ ]	CIN	-	15	pF
Input capacitance [CKE0]	CCKE	-	15	pF
Input capacitance [CLK0]	CCLK	-	23	pF
Input capacitance [ $\overline{\text{CS0}}$ , $\overline{\text{CS2}}$ ]	CCS	-	15	pF
Input capacitance [DQM0 - DQM7]	CDQM	-	15	pF
Data input/output capacitance[DQ0 - DQ63]	COUT <sup>1</sup>	-	16	pF
Check bits [CB0 - 7]	COUT <sup>2</sup>	-	16	pF



**8M X 72 SDRAM DIMM with PLL and Register, based on 8M X 8, 4 Banks, 4K Refresh, 3.3V Synchronous DRAMs WITH SPD**

**DC AND OPERATING CHARACTERISTICS** (Recommended operating conditions unless otherwise noted) T A = 0 to 70°C

Symbol	Test Condition	Version	Unit
		-75	
ICC1 <sup>1</sup>	Burst Length = 1 tRC ≥ tRC (min) IOL = 0mA	1,175	mA
ICC2P <sup>3</sup>	CKE ≤ VIL (max), tCC = 10ns	359	mA
ICC2PS <sup>3</sup>	CKE & CLK ≤ VIL (max), tCC = ∞	11	
ICC2N <sup>3</sup>	CKE VIH (min), $\overline{CS} \geq VIH$ (min), tCC = 10ns Input signals are changed one time during 20ns	485	mA
ICC2NS <sup>3</sup>	CKE ≥ VIH (min), CLK ≤ VIL (max), tCC = ∞ Input signals are stable	56	
ICC3P <sup>3</sup>	CKE ≤ VIL (max), tCC = 10ns	377	mA
ICC3PS <sup>3</sup>	CKE & CLK ≤ VIL (max), tCC = ∞	29	
ICC3N <sup>3</sup>	CKE VIH (min), $\overline{CS} \geq VIH$ (min), tCC = 10ns Input signals are changed one time during 20ns	575	mA
ICC3NS <sup>3</sup>	CKE ≥ VIH (min), CLK ≤ VIL (max), tCC = ∞ Input signals are stable	137	
ICC4 <sup>1</sup>	IOL = 0mA Page Burst 4 Banks activated tCCD = 2CLKS	1,535	mA
ICC5 <sup>2</sup>	tRC tRC (min)	1,715	mA
ICC6 <sup>3</sup>	CKE ≤ 0.2V	359	mA

- ICC1: Operating Current (one bank active)
- ICC2P: Precharge Standby Current in power-down mode
- ICC2PS: Precharge Standby Current in power-down mode.
- ICC2N: Precharge Standby Current in non power-down mode.
- ICC2NS: Precharge Standby Current in non power-down mode.
- ICC3P: Active Standby Current in power-down mode.
- ICC3PS: Active Standby Current in power-down mode.
- ICC3N: Active Standby Current in non power-down mode (One Bank Active).
- ICC3NS: Active Standby Current in non power-down mode (One Bank Active).
- ICC4: Operating Current (Burst Mode)
- ICC5: Refresh Current
- ICC6: Self Refresh Current

**Notes:**

1. Measured with outputs open.
2. Refresh period is 64ms.
3. Measured with 1 PLL & 2 Drive ICs.
4. Unless otherwise noted, input swing level is CMOS(VIH/VIL=VDDQ/VSSQ).



**8M X 72 SDRAM DIMM with PLL and Register, based on 8M X 8, 4 Banks, 4K Refresh, 3.3V Synchronous DRAMs WITH SPD**

**AC OPERATING TEST CONDITIONS** (VDD = 3.3V ± 0.3V, TA = 0 to 70°C)

Parameter	Value
AC input levels	V <sub>IH</sub> /V <sub>IL</sub> = 2.4V / 0.4V
Input timing measurement reference level	1.4V
Input rise and fall time	t <sub>r</sub> / t <sub>f</sub> = 1ns / 1ns
Output measurement reference level	1.4V
Output load condition	See Fig. 2

**OPERATING AC PARAMETER** (AC operating conditions unless otherwise noted)

Refer to the individual component not the whole module.

Parameter	Symbol	Version	Unit	Note
		-75		
Row Active to Row Active delay	t <sub>RRD</sub> (min)	15	ns	1
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay	t <sub>RCD</sub> (min)	20	ns	1
Row precharge time	t <sub>RP</sub> (min)	20	ns	1
Row active time	t <sub>RAS</sub> (min)	45	ns	1
	t <sub>RAS</sub> (max)	100	us	-
Row cycle time	t <sub>RC</sub> (min)	65	ns	1
Last data in to row precharge	t <sub>RDL</sub> (min)	2	CLK	2
Last data in to Active delay	t <sub>DAL</sub> (min)	2CLK + 20 ns	-	-
Last data in to new col. add. delay	t <sub>CDL</sub> (min)	1	CLK	2
Last data in to burst stop	t <sub>BDL</sub> (min)	1	CLK	2
Column address to col. add. delay	t <sub>CCD</sub> (min)	1	CLK	3
Number of valid output data	CAS latency = 3	2	ea	4
	-	-	-	-

- Note :
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
  2. Minimum delay is required to complete write.
  3. All parts allow every cycle column address change.
  4. In case of row precharge interrupt, auto precharge and read burst stop.

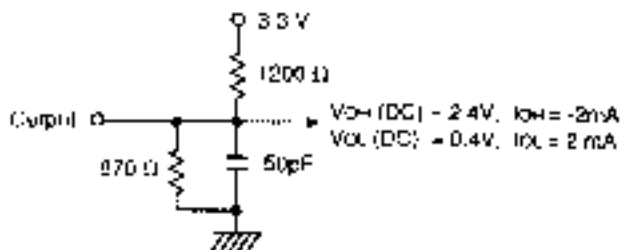


Fig. 1: DC Output Load Circuit

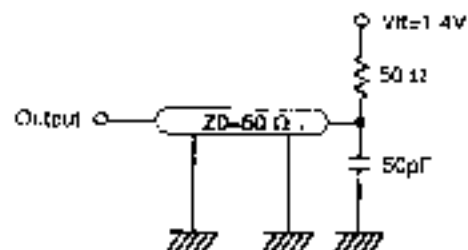


Fig. 2: AC Output Load Circuit



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**AC CHARACTERISTICS** (AC Operating conditions unless otherwise noted)  
Refer to the individual component, not the whole module.

Parameter	Symbol	-75		Unit	Note
		Min	Max		
CLK cycle time	tCC	7.5	1000	ns	1
CLK to valid output delay	tSAC		5.4	ns	1,2
Output data hold time	tOH	3.0		ns	1,2
CLK high pulse width	tCH	2.5		ns	3
CLK low pulse width	tCL	2.5		ns	3
Input setup time	tSS	1.5		ns	3
Input hold time	tSH	0.8		ns	3
CLK to output in Low-Z	tSLZ	1		ns	2
CLK to output in Hi-Z	tSHZ		5.4	ns	

- Note:
- Parameters depend on programmed CAS latency.
  - If clock rising time is no longer than 1ns,  $(tr/2-0.5)ns$  should be added to the parameter.
  - Assumed input rise and fall time ( $tr$  &  $tf$ ) = 1ns.  
If  $tr$  &  $tf$  is longer than 1ns, transient time compensation should be considered, i.e.,  $[(tr + tf)/2 - 1]$  ns should be added to the parameter.



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### SIMPLIFIED TRUTH TABLE

COMMAND		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9-A0	Note	
Register	Mode Register Set	H	X	L	L	L	L	X	OP CODE			1, 2	
Refresh	Auto Refresh	H	H	L	L	L	H	X	X			3	
	Self Refresh		Entry									L	3
	Refresh	Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Address		H	X	L	L	H	H	X	V	Row Address			
Read & Column Address	Auto Precharge Disable	H	X	L	H	L	H	X	V	L	Column Address (A0-A8)	4	
	Auto Precharge Enable									H		4, 5	
Write & Column Address	Auto Precharge Disable	H	X	L	H	L	L	X	V	L	Column Address (A0-A8)	4	
	Auto Precharge Enable									H		4, 5	
Burst Stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank Selection	H	X	L	L	H	L	X	V	L	X		
	All Banks								X	H			
Clock Suspend or Active Power Down	Entry	H	L	H	X	X	X	X	X				
				L	V	V	V						
	Exit	L	H	X	X	X	X	X					
Precharge Power Down Mode	Entry	H	L	H	X	X	X	X	X				
				L	H	H	H						
	Exit	L	H	H	X	X	X	X	X				
				L	V	V	V						
DQM		H				X			V	X		7	
No Operation Command		H	X	H	X	X	X	X	X				
				L	H	H	H						

(V = Valid, X = Don't Care, H = Logic High, L = Logic Low)

- Note:**
- OP Code: Operand Code  
A0 - A11, BA0 - BA1: Program keys. (@MRS)
  - MRS can be issued only at all banks precharge state.  
A new command can be issued after 2 clock cycles of MRS.
  - Auto refresh functions are same as CBR refresh of DRAM.  
The automatic precharge without row precharge command is meant by "Auto".  
Auto/self refresh can be issued only at all banks precharge state.
  - BA0 - BA1: Bank select addresses.  
If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.  
If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.  
If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.  
If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.  
If A10/AP is "High" at row precharge, BA0 and BA1 are ignored and all banks are selected.
  - During burst read or write with auto precharge, new read/write command can not be issued.  
Another bank read/write command can be issued after the end of burst.  
New row active of the associated bank can be issued at tRP after the end of burst.
  - Burst stop command is valid at every burst length.
  - DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0) but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)



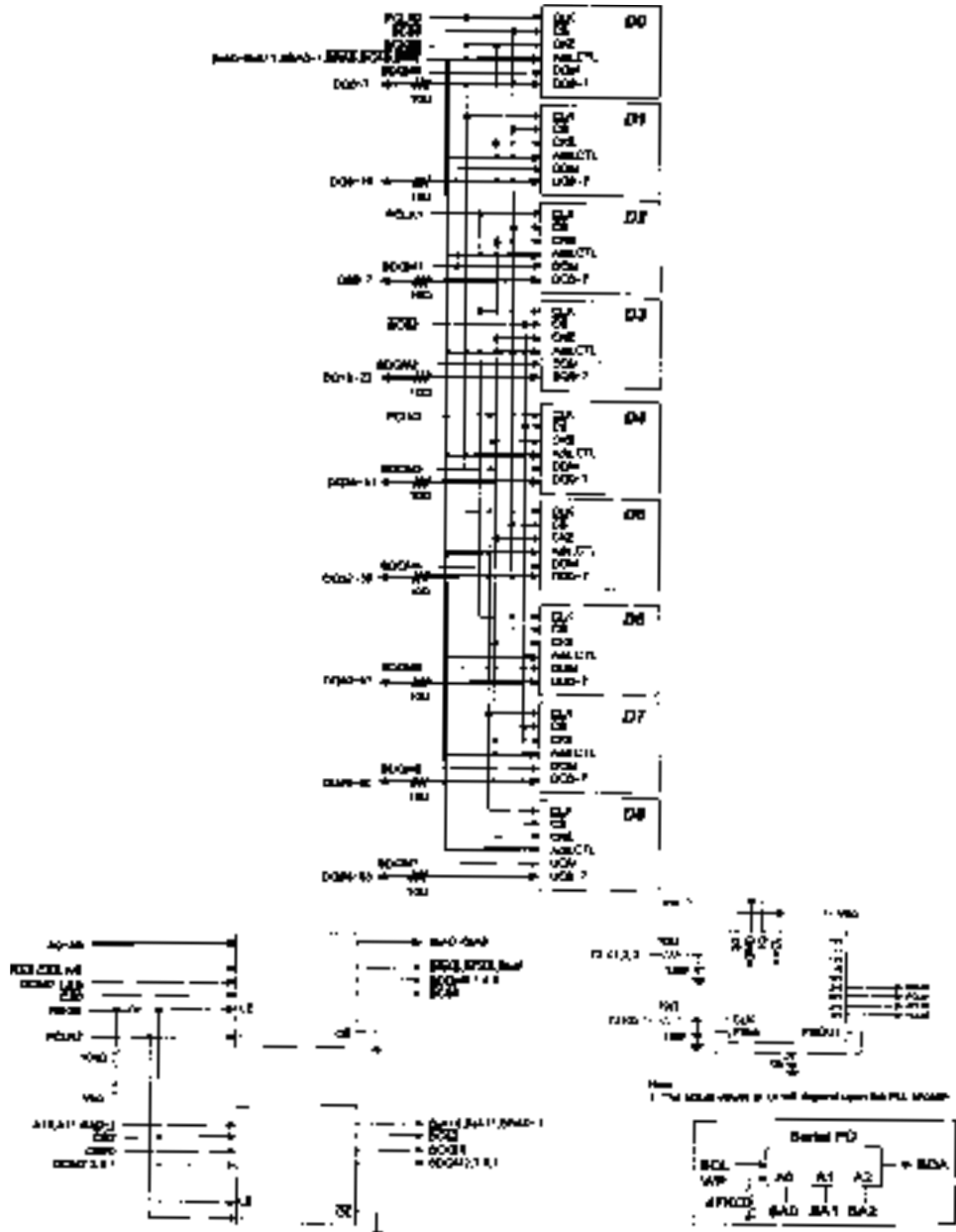
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FUNCTIONAL BLOCK DIAGRAM





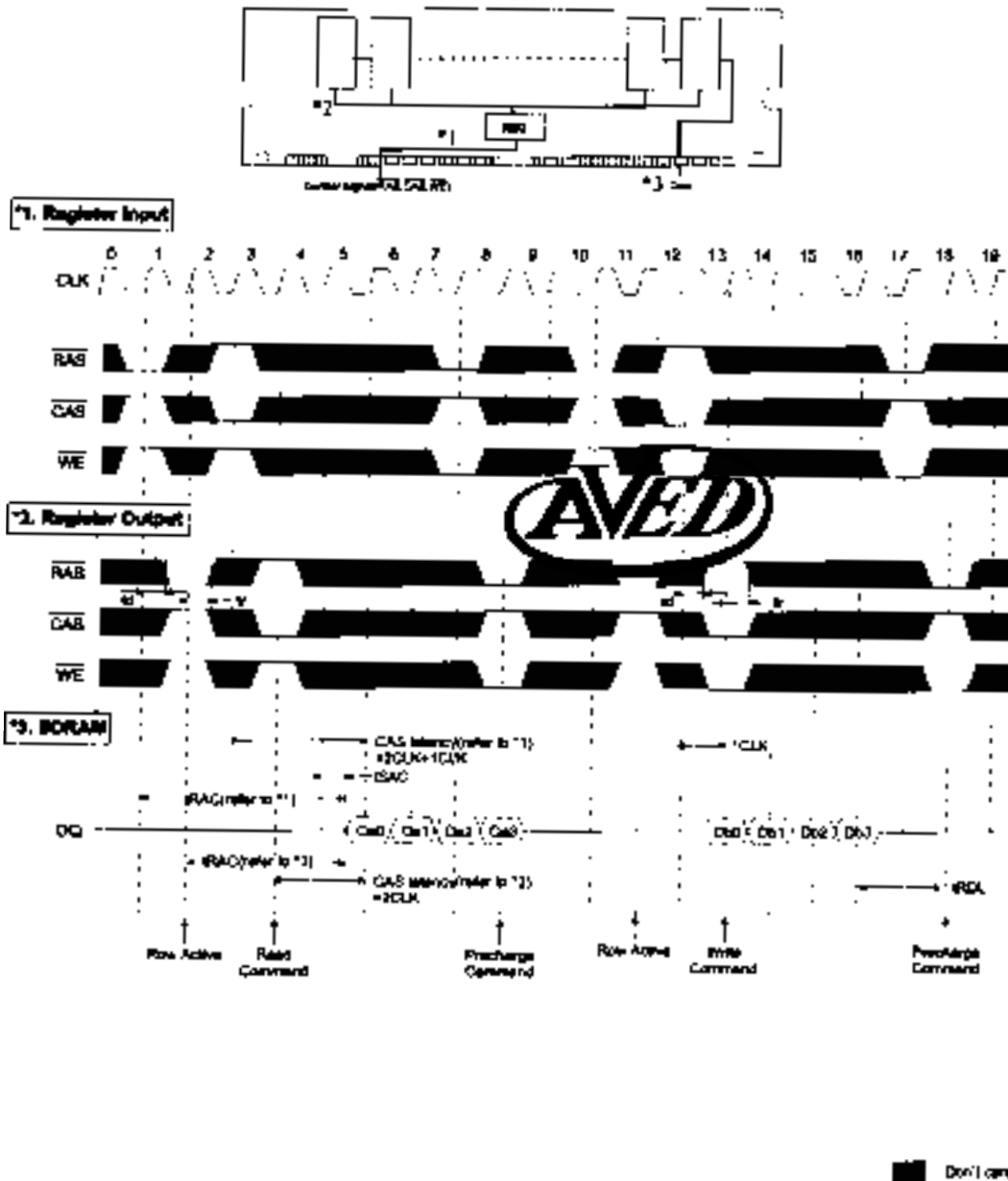
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### STANDARD TIMING DIAGRAM WITH PLL & REGISTER (CL=2, BL=4)



td, tr=Delay of register

- Notes:
1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register. Therefore, Input/Output signals of read/write function should be issued 1 CLK earlier as compared to Unbuffered DIMMS.
  2. DIN is to be issued 1 clock after write command in external timing because DIN is issued directly to module.



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### SERIAL PRESENCE DETECT

- Organization: 8M X 72
- Composition: 8M X 8\*9
- # of rows in module: 1
- # of banks in component: 4
- Refresh: 4K/64ms

Byte#	Function Description	Function Supported	Hex Value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	9	09h	1
5	# of module rows on this assembly	1	01h	
6	Data width of this assembly	72 bits	48h	
7	Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTTL	01h	
9	SDRAM cycle time @ CAS latency 3	7.5ns	75h	2
10	SDRAM access time from clock @ CAS latency 3	5.4ns	54h	2
11	DIMM configuration type	ECC	02h	
12	Refresh rate and type	15.625 $\mu$ s. support self refresh	80h	
13	Primary SDRAM width	X8	08h	
14	Error checking SDRAM width	X8	08h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes: Burst lengths supported	1,2,4,8 & Full page	8Fh	
17	SDRAM device attributes: # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes: CAS latency	3	04h	
19	SDRAM device attributes: CS latency	0 CLK	01h	
20	SDRAM device attributes: Write latency	0 CLK	01h	
21	SDRAM module attributes	Registered, Buffered DQM, address & control inputs and On-card PLL	16h	
22	SDRAM device attributes: General	$\pm$ 10% voltage tolerance, Burst Read, Single bit Write, precharge all. auto precharge	0Eh	
23	SDRAM cycle time @ CAS latency 2	-	00h	2
24	SDRAM access time @ CAS latency 2	-	00h	2
25	SDRAM cycle time @ CAS latency 1	-	00h	2
26	SDRAM access time @ CAS latency 1	-	00h	2
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module row density	1 row of 64MB	10h	
32	Command and address signal input setup time	1.5ns	15h	
33	Command and address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	
35	Data signal input hold time	0.8ns	08h	
36-61	Superset information (may be used in the future)	-	00h	



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### SERIAL PRESENCE DETECT (CONTINUED FROM PREVIOUS PAGE)

Byte#	Function Description	Function Supported	Hex Value	Note
		-75	-75	
62	SPD data revision code	JEDEC 2	02h	
63	Check sum for bytes 0-62	-	BDh	
64	Manufacturer JEDEC ID code	AVED Memory Products	67h	
65-71	Manufacturer JEDEC ID code	AVED Memory Products	00h	
72	Manufacturing location	Tustin	01h	
73	Manufacturer part #	A	41h	
74	Manufacturer part #	M	4Dh	
75	Manufacturer part #	P	50h	
76	Manufacturer part #	3	33h	
77	Manufacturer part #	7	37h	
78	Manufacturer part #	7	37h	
79	Manufacturer part #	P	50h	
80	Manufacturer part #	0	30h	
81	Manufacturer part #	8	38h	
82	Manufacturer part #	2	32h	
83	Manufacturer part #	3	33h	
84	Manufacturer part #	B	42h	
85	Manufacturer part #	T	54h	
86	Manufacturer part #	2	32h	
87	Manufacturer part #	-	2Dh	
88	Manufacturer part #	C	43h	
89	Manufacturer part #	7	37h	
90	Manufacturer part #	5	35h	
91	Manufacturer part #	/	2Fh	
92	Manufacturer part #	H	48h	
93	Manufacturer part #		20h	
94	Manufacturer revision code (for PCB)	2	32h	
95	Manufacturer revision code (for component)	D-die(5 <sup>th</sup> Gen.)	44h	
96	Manufacturing date (Week)	-	-	3
97	Manufacturing date (Year)	-	-	3
98-101	Assembly serial #	-	-	4
102-125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Reserved	133MHz	64h	
127	Reserved	CLK0, CL-3, ConAP	85h	

**Notes:**

1. The row select address is excluded in counting the total # of Addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date, Week & Date, Year with BCD format.
4. These bytes are programmed by AVED's own assembly serial # system. All modules may have different unique serial #s.
5. These bytes are Undefined and can be used for AVED's own purpose.