



AVED MEMORY PRODUCTS

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AVED16F664LSD17-60

16M X 64 DRAM SODIMM, EDO MODE, Using 8M X 16, 4K Refresh, 3.3V

DESCRIPTION

The AVED Memory Products AVED16F664LSD17-60 is a 16M bit X 64 Dynamic RAM high density memory module. The AVED Memory Products AVED16F664LSD17-60 consists of sixteen CMOS 8M X 16 bit DRAMs in TSOP 400mil package and a 2K EEPROM in 8-pin TSSOP package mounted on a 144-pin glass-epoxy substrate. A 0.1uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The AVED Memory Products AVED16F664LSD17-60 is a Dual in-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

APPLICATION

Main Memory unit for computer, Microcomputer memory, Refresh memory for CRT.

FEATURES

• Performance Ranges

Speed	tRAC	tCAC	tHPC
-6	60ns	15ns	25ns

• Part Identification

- AVED16F664LSD17-60
4K cycles/64ms, TSOP
- (XX = -6)

- Extended Data Out Mode operation
- New JEDEC standard proposal with EEPROM
- Serial Presence Detect with EEPROM
- \overline{CAS} before \overline{RAS} refresh capability
- Self-refresh capability
- \overline{RAS} -only and hidden refresh capability
- LVTTTL compatible inputs and outputs
- Single +3.3V \pm 0.3 power supply

Pin Names

Pin Names	Function
A0 - A11	Address Inputs
DQ0 - DQ63	Data In/Out
$\overline{W}0$ - $\overline{W}2$	Read/Write Enable
$\overline{OE}0$ - $\overline{OE}2$	Output Enable
RAS0 - RAS3	Row Address Strobe
$\overline{CAS}0$ - $\overline{CAS}7$	Column Address Strobe
Vcc	Power (+3.3V)
Vss	Ground
SDA	Serial PD/Data I/O
SCL	Serial PD Clock Input
SA0 - SA2	Serial PD Address Input



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PIN CONFIGURATIONS (FRONT SIDE / BACK SIDE)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	49	DQ13	50	DQ45	97	DQ22	98	DQ54
3	DQ0	4	DQ32	51	DQ14	52	DQ46	99	DQ23	100	DQ55
5	DQ1	6	DQ33	53	DQ15	54	DQ47	101	Vcc	102	Vcc
7	DQ2	8	DQ34	55	Vss	56	Vss	103	A6	104	A7
9	DQ3	10	DQ35	57	NC	58	NC	105	A8	106	A11
11	Vcc	12	Vcc	59	NC	60	NC	107	Vss	108	Vss
13	DQ4	14	DQ36	61	NC	62	NC	109	A9	110	NC
15	DQ5	16	DQ37	63	Vcc	64	Vcc	111	A10	112	NC
17	DQ6	18	DQ38	65	NC	66	NC	113	Vcc	114	Vcc
19	DQ7	20	DQ39	67	\overline{W}	68	NC	115	$\overline{CAS2}$	116	$\overline{CAS6}$
21	Vss	22	Vss	69	$\overline{RAS0}$	70	NC	117	$\overline{CAS3}$	118	$\overline{CAS7}$
23	$\overline{CAS0}$	24	$\overline{CAS4}$	71	$\overline{RAS1}$	72	NC	119	Vss	120	Vss
25	$\overline{CAS1}$	26	$\overline{CAS5}$	73	\overline{OE}	74	NC	121	DQ24	122	DQ56
27	Vcc	28	Vcc	75	Vss	76	Vss	123	DQ25	124	DQ57
29	A0	30	A3	77	NC	78	NC	125	DQ26	126	DQ58
31	A1	32	A4	79	NC	80	NC	127	DQ27	128	DQ59
33	A2	34	A5	81	Vcc	82	Vcc	129	Vcc	130	Vcc
35	Vss	36	Vss	83	DQ16	84	DQ48	131	DQ28	132	DQ60
37	DQ8	38	DQ40	85	DQ17	86	DQ49	133	DQ29	134	DQ61
39	DQ9	40	DQ41	87	DQ18	88	DQ50	135	DQ30	136	DQ62
41	DQ10	42	DQ42	89	DQ19	90	DQ51	137	DQ31	138	DQ63
43	DQ11	44	DQ43	91	Vss	92	Vss	139	Vss	140	Vss
45	Vcc	46	Vcc	93	DQ20	94	DQ52	141	SDA	142	SCL
47	DQ12	48	DQ44	95	DQ21	96	DQ53	143	Vcc	144	Vcc



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ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.5 to + 4.6	V
Voltage on Vcc supply relative to Vss	V _{cc}	-0.5 to + 4.6	V
Storage Temperature	T _{stg}	-55 to + 125	°C
Power Dissipation	P _d	16	W
Short Circuit Output Current	IOS	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, Ta = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{cc}	3.0	3.3	3.6	V
Ground	V _{ss}	0	0	0	V
Input High Voltage	V _{IH}	2.0	-	V _{cc} +0.3*	V
Input Low Voltage	V _{IL}	- 0.3**	-	0.8	V

*1: V_{cc}+ 1.3V/15ns, Pulse width is measured at V_{cc}.

**2: -1.3V/15ns, Pulse width is measured at V_{ss}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	AVED16F664LSD17-60		Unit
		Min	Max	
ICC	-6	-	2240	mA
ICC2	-	-	16	mA
ICC3	-6	-	2240	mA
ICC4	-6	-	1120	mA
ICC5	-	-	30	mA
ICC6	-6	-	2240	mA
ICC7	-	-	10	mA
ICC8	-	-	11.2	mA
I _I (L)	-	-10	10	µA
I _O (L)	-	-5	5	µA
VOH	-	2.4	-	V
VOL	-	-	0.4	V

ICC1: Operating Current * (\overline{RAS} , \overline{CAS} , Address cycling @tRC=min.)

ICC2: Standby Current ($\overline{RAS} = \overline{CAS} = \overline{W} = V_{IH}$)

ICC3: \overline{RAS} Only Refresh Current * ($\overline{CAS} = V_{IH}$, \overline{RAS} cycling @tRC = min.)

ICC4: EDO Mode Current * ($\overline{RAS} = V_{IL}$, \overline{CAS} address cycling: tHPC=min.)

ICC5: Standby Current ($\overline{RAS} = \overline{CAS} = \overline{W} = V_{cc}-0.2V$)

ICC6: \overline{CAS} -Before- \overline{RAS} Refresh Current * (\overline{RAS} and \overline{CAS} cycling @ tRC = min.)

ICC7: Battery back-up current. Average power supply, Battery back-up mode.
Input high voltage(V_{IH})=V_{CC}-0.2V, Input low voltage(V_{IL})=0.2V, \overline{CAS} =0.2V.
tRC=31.25us, tRAS=tRASmin~300ns.

ICCS: Self-Refresh Current, $\overline{RAS}=\overline{CAS}=V_{IL}$, $\overline{W}=\overline{OE}=A0-A11=V_{cc}-0.2V$ or 0.2V, DQ-DQ63=V_{cc}-0.2V or Open

I_I(L): Input Leakage Current (Any input 0 ≤ V_{IN} ≤ V_{cc}+0.3V, all other pins not under test = 0V.)

I_O(L): Output Leakage Current (Data out is disabled, 0V ≤ V_{out} ≤ V_{cc})

VOH: Output High Voltage Level (I_{OH} = -2mA)

VOL: Output Low Voltage Level (I_{OL} = 2mA)

*NOTE: ICC1, ICC3, ICC4 and ICC6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. ICC is specified as an average current. In ICC1, ICC3 and ICC6, address can be changed maximum once while $\overline{RAS} = V_{IL}$. In ICC4, address can be changed maximum once within one EDO mode cycle, tHPC.



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CAPACITANCE (Ta = 0 - 70 °C, f=1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance [A0 - A11]	CIN1	-	95	pF
Input capacitance [$\overline{WE}0$ - $\overline{WE}2$, $\overline{OE}0$ - $\overline{OE}2$]	CIN2	-	70	pF
Input capacitance [$\overline{RAS}0$ - $\overline{RAS}3$]	CIN3	-	40	pF
Input capacitance [$\overline{CAS}0$ - $\overline{CAS}7$]	CIN4	-	24	pF
Input/Output capacitance [DQ0 - 63]	CDQ	-	18	pF

AC CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, Vcc=3.3V ± 0.3V, Vss=0V)

Test condition: Vih/Vil=2.2/0.7V, Voh/Vol=2.0V/0.8V, Output loading CL = 100pF

STANDARD OPERATION	Symbol	Min	- 60 Max	Unit	Notes
Random read or write cycle time	tRC	110		ns	
Read-modify-write cycle time	tRWC	140		ns	
Access time from \overline{RAS}	tRAC		60	ns	4,5,10,11
Access time from \overline{CAS}	tCAC		15	ns	4,5,10
Access time from column address	tAA		30	ns	4,5,11
\overline{CAS} to output in Low-Z	tCLZ	0		ns	3
Output buffer turn-off delay from \overline{CAS}	tCEZ	0	15	ns	
Transition time (rise and fall)	tT	2	50	ns	4
\overline{RAS} precharge time	tRP	40		ns	
\overline{RAS} pulse width	tRAS	60	10K	ns	
\overline{RAS} hold time	tRSH	15		ns	
\overline{CAS} hold time	tCSH	55		ns	
\overline{CAS} pulse width	tCAS	10	10K	ns	
RAS to \overline{CAS} delay time	tRCD	20	45	ns	10
\overline{RAS} to column address delay time	tRAD	15	30	ns	11
\overline{CAS} to \overline{RAS} precharge time	tCRP	5		ns	
\overline{CAS} precharge time	tCP	10		ns	
Row address set-up time	tASR	0		ns	
Row address hold time	tRAH	10		ns	
Column address set-up time	tASC	0		ns	
Column address hold time	tCAH	10		ns	
Column address hold time ref. to \overline{RAS}	tAR	50		ns	
Column address to \overline{RAS} lead time	tRAL	30		ns	
Read command set-up time	tRCS	0		ns	
Read command hold time ref. to \overline{CAS}	tRCH	0		ns	7
Read command hold time ref. to \overline{RAS}	tRRH	0		ns	7
Write command set-up time	tWCS	0		ns	9
Write command hold time	tWCH	10		ns	
Write command pulse width	tWP	10		ns	
Write command hold time from \overline{RAS}	tWCR	45		ns	



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AC CHARACTERISTICS (continued)

STANDARD OPERATION	Symbol	-60		Unit	Notes
		Min	Max		
Write command to $\overline{\text{RAS}}$ lead time	tRWL	15		ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	10		ns	
Data set-up time	tDS	0		ns	8
Data hold time	tDH	10		ns	8
Refresh period (4K)	tREF		64	ms	12
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tCWD	36		ns	9
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	tRWD	80		ns	9
Column address to $\overline{\text{W}}$ delay time	tAWD	50		ns	9
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ - before - $\overline{\text{RAS}}$ refresh)	tCSR	5		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ - before - $\overline{\text{RAS}}$ refresh)	tCHR	10		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	tRPC	5		ns	
Access time from $\overline{\text{CAS}}$ precharge	tCPA		35	ns	4
Hyper Page mode cycle time	tHPC	25		ns	
Hyper Page mode read-modify-write cycle	tHPRWC	60		ns	
$\overline{\text{CAS}}$ Precharge Time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ counter test)	tCPT	30		ns	
$\overline{\text{RAS}}$ Hold Time referenced to $\overline{\text{OE}}$	tROH	0		ns	
$\overline{\text{RAS}}$ pulse width (EDO mode)	tRASP	60	100K	ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ precharge time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ refresh)	tWRP	10		ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ hold time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ refresh)	tWRH	10		ns	
$\overline{\text{OE}}$ access time	tOEA		15	ns	
$\overline{\text{OE}}$ to data delay	tOED	15		ns	
$\overline{\text{OE}}$ command hold time	tOEH	15		ns	
$\overline{\text{OE}}$ to $\overline{\text{CAS}}$ hold time	tOCH	5		ns	
$\overline{\text{CAS}}$ hold time to $\overline{\text{OE}}$	tCHO	5		ns	
$\overline{\text{OE}}$ precharge time	tOEP	5		ns	
Output buffer turn off delay time from $\overline{\text{OE}}$	tOEZ	0	15	ns	6
Output data hold time	tDOH	5		ns	
Output buffer turn off delay from $\overline{\text{RAS}}$	tREZ	0	15	ns	6
Output buffer turn off delay from $\overline{\text{W}}$	tWEZ	0	15	ns	6
$\overline{\text{w}}$ to data delay	tWED	15		ns	
$\overline{\text{w}}$ pulse width (EDO cycle)	tWPE	5		ns	
$\overline{\text{RAS}}$ pulse width ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ self-refresh)	tRASS	100		us	
$\overline{\text{RAS}}$ precharge time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ self-refresh)	tRPS	100		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ self-refresh)	tCHS	-50		ns	
$\overline{\text{W}}$ delay time from $\overline{\text{CAS}}$ precharge	tCPWD	54		ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	tRHCP	35		ns	
Write command set-up time (test mode)	tWTS	10		ns	
Write command hold time (test mode)	tWTH	10		ns	



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NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 \overline{RAS} -only or \overline{CAS} -before- \overline{RAS} refresh cycles before proper device operation is achieved.
2. Input voltage levels are VIH/VIL. VIH(min) and VIL(max) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min) and VIL(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1TTL load and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, access time is controlled exclusively by tCAC.
5. Assumes that tRCD \geq tRCD(max).
6. tWCS, tRWD, tCWD, tAWD, and tCPWD are non-restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS \geq tWCS(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If tRWD \geq tRWD(min), tCWD \geq tCWD(min), tAWD \geq tAWD(min) and tCPWD \geq tCPWD(min), the cycle is a read-modify-write cycle and the data out will contain data read from the selected address. If neither of the above sets of conditions is satisfied, the condition of data out (at access time) is indeterminate.
7. Either tRCH or tRRH must be satisfied for a read cycle.
8. These parameters are referenced to the \overline{CAS} leading edge in early write cycles.
9. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, access time is controlled by tAA.
10. tASC \geq 6ns, assume tT=2.0ns.
11. For all the refresh modes except distributed \overline{CAS} -before- \overline{RAS} refresh, 4096 cycles of burst refresh must be executed within 16ms before and after self-refresh in order to meet refresh specifications.
12. If \overline{RAS} goes high before \overline{CAS} goes high, the open circuit condition of the output is achieved by \overline{CAS} going high. If \overline{CAS} goes high before \overline{RAS} goes high, the open circuit condition of the output is achieved by \overline{RAS} going high.



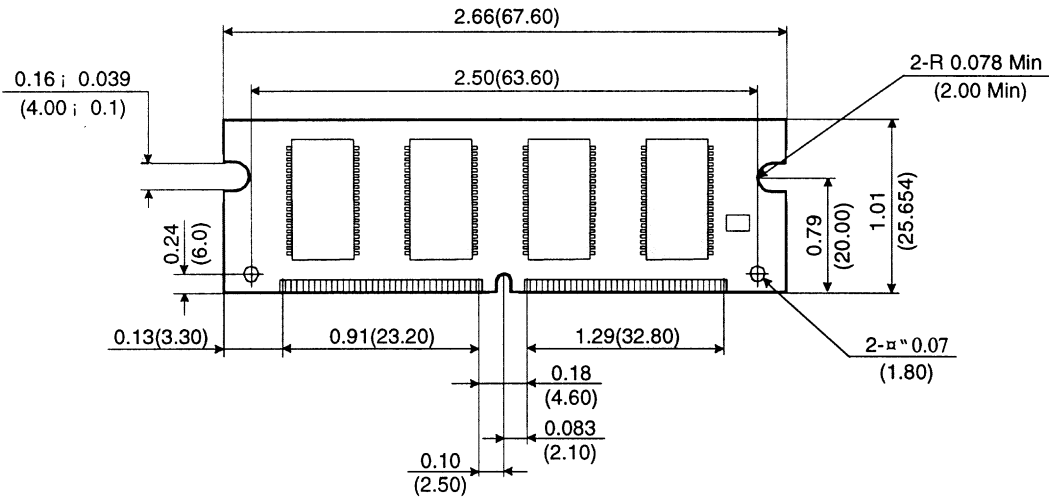
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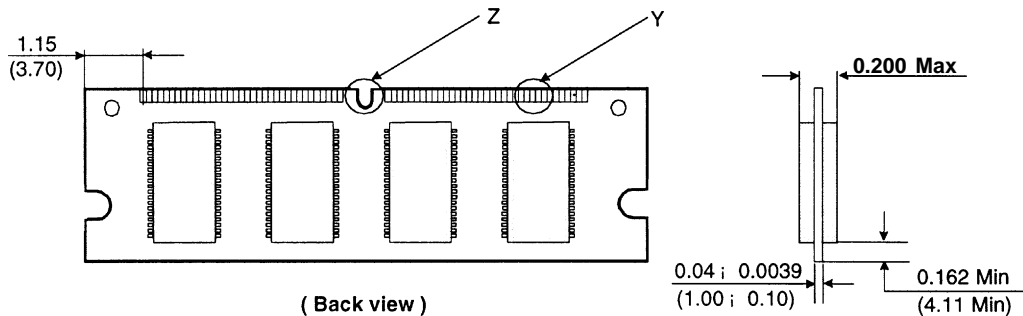
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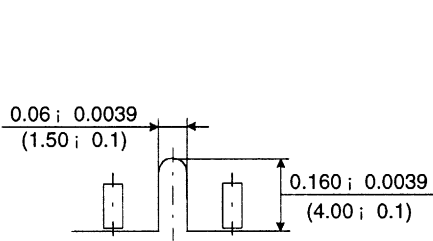
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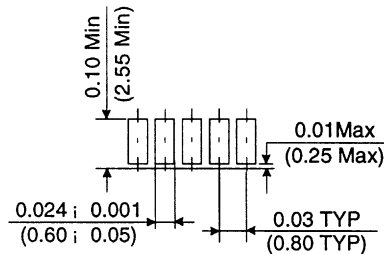
(Front view)



(Back view)



Detail Z



Detail Y

Aved Memory Products reserves the right to change products and specifications without notice