AVED MEMORY PRODUCTS

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AVED1F321SDMW/LDMW
AVED1F324SDMW/LDMW

FAST PAGE MODE WITH EDO, 1MX32 DRAM DIMM, 1MX16, 1K & 4K REFRESH, 3.3V

DESCRIPTION

AVED Memory Products AVED1F32*SDMW/LDMW (1,4) is a 1M bit x 32 Dynamic RAM high density memory module. The AVED Memory Products AVED1F32*SDMW/LDMW (1,4) consists of two CMOS 1Mx16bit DRAMs in 44-pin TSOPII packages mounted on a 72-pin six layer zigzag glass-epoxy substrate. A 0.22uf decoupling capacitor is mounted on the printed circuit board for each DRAM. The AVED Memory Products AVED1F32*SDMW/LDMW (1, 4) is a Dual In-Line Memory Module with edge connections and is intended for mounting into 72 pin dual readout zigzag edge connector sockets.

APPLICATION

Main Memory unit for computer, Microcomputer memory, Refresh memory for CRT.

FEATURES

- **Performance Ranges**

Speed	tRAC	tCAC	tRC	tHPC
-60	60ns	17ns	110ns	30ns
-70	70ns	20ns	130ns	33ns

- Part Identification
  - AVED1F321SDMW-XX
    1024 cycles/16ms Ref, TSOP, Tin Contact Plating
  - AVED1F321LDMW-XX
    1024 cycles/16ms Ref, TSOP, Gold Contact Plating
  - AVED1F324SDMW-XX
    4096 cycles/16ms Ref, TSOP, Tin Contact Plating
  - AVED1F324LDMW-XX
    4096 cycles/16ms Ref, TSOP, Gold Contact Plating
  - (XX= -60, -70)
- Fast Page with EDO Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self refresh capability
- TTL compatible inputs and outputs
- Single +3.3V $\pm$ 0.3V power supply

PIN NAMES

A0 - A9	Address Inputs (1K Ref)
A0 - A11	Address Inputs (4K Ref)
DQ(0-7,9-16, 18-25,27-34)	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
PD1 - PD7	Presence Detect
Vdd	Power (+3.3V)
Vss	Ground
NC	No Connection

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	Vss	37	DQ18
2	DQ0	38	DQ19
3	DQ1	39	Vss
4	DQ2	40	$\overline{CAS0}$
5	DQ3	41	$\overline{CAS2}$
6	DQ4	42	$\overline{CAS3}$
7	DQ5	43	$\overline{CAS1}$
8	DQ6	44	$\overline{RAS0}$
9	DQ7	45	NC
10	Vdd	46	NC
11	PD1	47	$\overline{W}$
12	A0	48	NC
13	A1	49	DQ20
14	A2	50	DQ21
15	A3	51	DQ22
16	A4	52	DQ23
17	A5	53	DQ24
18	A6	54	DQ25
19	A10	55	NC
20	NC	56	DQ27
21	DQ9	57	DQ28
22	DQ10	58	DQ29
23	DQ11	59	DQ31
24	DQ12	60	DQ30
25	DQ13	61	Vdd
26	DQ14	62	DQ32
27	DQ15	63	DQ33
28	A7	64	DQ34
29	A11	65	NC
30	Vdd	66	PD2
31	A8	67	PD3
32	A9	68	PD4
33	NC	69	PD5
34	$\overline{RAS2}$	70	PD6
35	DQ16	71	PD7
36	NC	72	Vss

PRESENCE DETECT PINS (Optional)

Pin	60NS	70NS
PD1	NC	NC
PD2	Vss	Vss
PD3	Vss(NC)	Vss(NC)
PD4	NC	NC
PD5	NC	NC
PD6	NC	NC
PD7	NC	NC

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ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V_{IN}, VOUT	-0.5 to +4.6	V
Voltage on Vdd supply relative to Vss	Vdd	-0.5 to +4.6	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	Pd	2	W
Short Circuit Output Current	IOS	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, Ta = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vdd	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input High Voltage	VIH	2.1	-	Vdd+0.3*1	V
Input Low Voltage	VIL	-0.3*2	-	0.8	V

*1: Vdd+1.3V/15ns (3.3V), Pulse width is measured at Vdd.
*2: -1.3V/15ns (3.3V), Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

		AVED1F321SDMW/LDMW		AVED1F324SDMW/LDMW		
Symbol	Speed	Min	Max	Min	Max	Unit
ICC1	-60	-	300	-	180	mA
	-70	-	280	-	160	mA
ICC2	-	-	2	-	2	mA
ICC3	-60	-	300	-	180	mA
	-70	-	280	-	160	mA
ICC4	-60	-	200	-	180	mA
	-70	-	180	-	160	mA
ICC5	-	-	400	-	400	uA
ICC6	-60	-	300	-	180	mA
	-70	-	280	-	160	mA
ICC7	-	-	800	-	800	µA
ICCS	-	-	400	-	400	µA
I1(L)	-	-10	10	-10	10	µA
I0(L)	-	-5	5	-5	5	µA
VOH	-	2.4	-	2.4	-	V
VOL	-	-	0.4	-		V

ICC1: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @tRC=min.)
ICC2: Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = $\overline{W}$ = VIH)
ICC3: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$ = VIH, $\overline{RAS}$ cycling @tRC = min.)
ICC4: EDO Mode Current * ($\overline{RAS}$ =VIL, $\overline{CAS}$ cycling : tHPC=min.)
ICC5: Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = $\overline{W}$ =Vdd-0.2V)
ICC6: $\overline{CAS}$ -Before- $\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @ tRC = min.)
ICC7: Battery Back-Up Current, Average power supply current, Battery back-up mode
Input High voltage (VIH)=Vcc-0.2V, Input Low Voltage (VIL)=0.2V, $\overline{CAS}$ =0.2V
DQ0-31=Don't Care, tRC=31.25µs(4K Ref), 125 µs(1K Ref), tRAS=tRASmin~300ns
ICCS: Self Refresh Current
$\overline{RAS}$ = $\overline{CAS}$ =VIL, $\overline{W}$ = $\overline{OE}$ =A0–A11=Vcc-0.2V or 0.2V, DQ0–DQ31=Vcc-0.2V, 0.2V or Open
I1(L): Input Leakage Current (Any input 0 ≤ VIN ≤ Vdd+0.3V, all other pins not under test = 0 V.)
I0(L): Output Leakage Current (Data out is disabled, 0V ≤ Vout ≤ Vdd)
VOH: Output High Voltage Level (IOH =-2mA)
VOL: Output Low Voltage Level (IOL =2mA)

* NOTE: ICC1, ICC3, ICC4 and ICC6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. ICC is specified as an average current. In ICC1 and ICC3, address can be changed maximum once while $\overline{RAS}$ =VIL. In ICC4, address can be changed maximum once within one EDO mode cycle, tHPC.

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CAPACITANCE (Ta = 25 °C, Vdd=3.3V, f=1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance [A0-A11 (A9)]	CIN1	-	25	pF
Input capacitance [$\overline{W}$]	CIN2	-	30	pF
Input capacitance [$\overline{RAS0}$, $\overline{RAS2}$]	CIN3	-	15	pF
Input capacitance [$\overline{CAS0}$ - $\overline{CAS3}$]	CIN4	-	15	pF
Input/Output capacitance [DQ0-7,9-16,18-25,27-34]	CDQ1	-	17	pF

AC CHARACTERISTICS (0°C ≤ Ta≤ 70°C, Vdd=3.3V ±0.3V. See notes 1,2.)
Test condition: Vih/Vil=2.1V/0.8V, Voh/Vil=2.0V/0.8V, Output loading CL=100pF

STANDARD OPERATION	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	Unit	Notes
Random read or write cycle time	tRC	110		130		ns	
Read-modify-write cycle time	tRWC	155		185		ns	
Access time from $\overline{RAS}$	tRAC		60		70	ns	3, 4, 10
Access time from $\overline{CAS}$	tCAC		17		20	ns	3, 4, 5
Access time from column address	tAA		30		35	ns	3, 10
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	3	15	3	20	ns	6, 11, 12
Transition time (rise and fall)	tT	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	40		50		ns	
$\overline{RAS}$ pulse width	tRAS	60	10K	70	10K	ns	
$\overline{RAS}$ hold time	tRSH	17		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		ns	
$\overline{CAS}$ pulse width	tCAS	10	10K	15	10K	ns	13
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	45	20	50	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	30	15	35	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		ns	
Row address set-up time	tASR	0		0		ns	
Row address hold time	tRAH	10		10		ns	
Column address set-up time	tASC	0		0		ns	
Column address hold time	tCAH	10		15		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		ns	
Read command set-up time	tRCS	0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		ns	8
Write command hold time	tWCH	10		15		ns	
Write command pulse width	tWP	10		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		ns	
Write command to $\overline{CAS}$ lead time	tCWL	10		15		ns	
Data set-up time	tDS	0		0		ns	9

AC CHARACTERISITICS (continued)

STANDARD OPERATION	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	Unit	Notes
Data hold time	tDH	10		15		ns	9
Refresh period	tREF		128		128	ms	
Write command set-up time	tWCS	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	40		50		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	85		95		ns	7
Column address to $\overline{W}$ delay time	tAWD	55		60		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	60		65		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$ -before- $\overline{RAS}$ refresh)	tCSR	5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ -before- $\overline{RAS}$ refresh)	tCHR	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$ -B- $\overline{R}$ counter test cycle)	tCPT	20		25		ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40	ns	3
Hyper Page cycle time	tHPC	30		33		ns	13
$\overline{CAS}$ precharge time (Hyper Page cycle)	tCP	10		10		ns	
$\overline{RAS}$ pulse width (Hyper Page cycle)	tRASP	60	200K	70	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	35		40		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$ -B- $\overline{R}$ refresh)	tWRP	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$ -B- $\overline{R}$ refresh)	tWRH	10		10		ns	
Output data hold time	tDOH	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	15	3	20	ns	6, 11, 12
Output buffer turn off delay from $\overline{W}$	tWEZ	3	15	3	20	ns	6, 11
$\overline{W}$ to data delay	tWED	15		20		ns	
$\overline{W}$ pulse width (Hyper Page Cycle)	tWPE	5		5		ns	
$\overline{RAS}$ pulse width ($\overline{C}$ -B- $\overline{R}$ self refresh)	tRASS	100		100		us	
$\overline{RAS}$ precharge time ($\overline{C}$ -B- $\overline{R}$ self refresh)	tRPS	110		130		ns	
$\overline{CAS}$ hold time ($\overline{C}$ -B- $\overline{R}$ self refresh)	tCHS	-50		-50		ns	

NOTES

1. An initial pause of 200µs is required after power-up followed by any 8 $\overline{RAS}$ -only or $\overline{CAS}$ -before- $\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. VIH (min) and VIL (max) are reference levels for measuring timing of input signals. Transition times are measured between VIH (min) and VIL (max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2TTL loads and 100pF.

4. Operation within the tRCD (max) limit insures that tRAC (max) can be met. tRCD (max) is specified as a reference point only. If tRCD is greater than the specified tRCD (max) limit, then access time is controlled exclusively by tCAC.

5. Assumes that tRCD ≥ tRCD (max)

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.

7. tWCS, tRWD, tCWD and tAWD is non-restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If tWCS ≥ tWCS (min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.

   If tCWD ≥tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminated.

8. Either tRCH or tRRH must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.

10. Operation within the tRAD (max) limit insures that tRAC (max) can be met. tRAD (max) is specified as a reference point only. If tRAD is greater than the specified tRAD (max) limit, then access time is controlled by tAA.

11. tCEZ(max), tREZ(max), tWEZ(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.

12. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.

13. tASC ≥ tCP(min)

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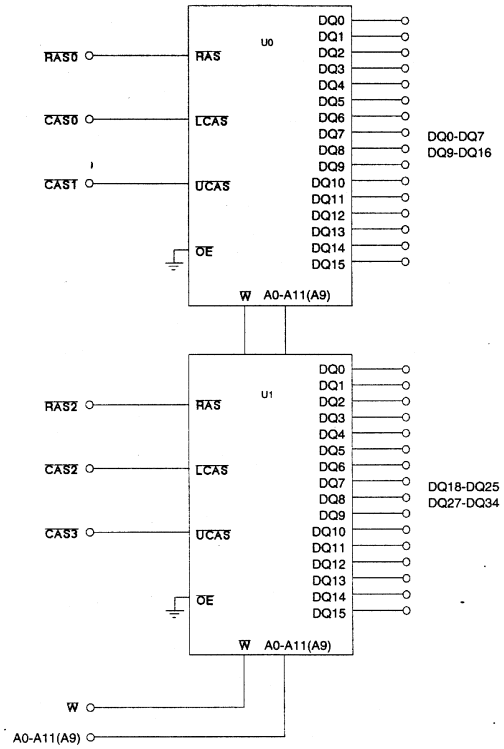
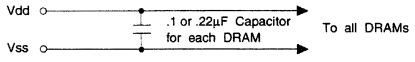
FUNCTIONAL BLOCK DIAGRAM





PACKAGE DIMENSIONS