



# AVED MEMORY PRODUCTS

Where Quality & Memory Merge

## AVED2M361JSQW-XX

FAST PAGE MODE, 2M X 36 SIMM Using 1M X 16 DRAM and 1M X 4 QUAD CAS DRAM, 1K REFRESH, 5V

### DESCRIPTION

AVED Memory Products AVED2M361JSQW-XX is a 2M bit X 36 Dynamic RAM high density memory module. The AVED Memory Products AVED2M361JSQW-XX consists of four CMOS 1M X16 bit DRAMs in 42-pin SOJ packages and two CMOS 1M X 4 bit Quad CAS DRAMs in 24-pin SOJ packages mounted on a 72-pin glass-epoxy substrate. A 0.1uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The AVED Memory Products AVED2M361JSQW-XX is a Single In-Line Memory Module with edge connections and is intended for mounting into 72-pin edge connector sockets.

### APPLICATION

Main Memory unit for computer, Microcomputer memory, Refresh memory for CRT.

### FEATURES

- Performance Ranges

Speed	tRAC	tCAC	tRC	tHPC
-60	60ns	17ns	110ns	30ns

- Part Identification
  - AVED2M361JSQW-XX  
1024 cycles/16ms Ref, SOJ, Tin Contact Plating
- [XX= -60]
- Fast Page Mode Operation
- CAS-before-RAS refresh capability
- RAS-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single +5V ± 10% power supply
- JEDEC standard PDPin & pinout

### PIN NAMES

A0 - A9	Address Inputs
DQ0 - DQ35	Data In/Out
$\overline{W}$	Read/Write Input
RAS0 - RAS3	Row Address Strobe
CAS0 - CAS3	Column Address Strobe
PD1 - PD4	Presence Detect
Vcc	Power (+5V)
Vss	Ground
NC	No Connection
Res	Reserved Pin

### PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	Vss	37	DQ17
2	DQ0	38	DQ35
3	DQ18	39	Vss
4	DQ1	40	CAS0
5	DQ19	41	CAS2
6	DQ2	42	CAS3
7	DQ20	43	CAS1
8	DQ3	44	RAS0
9	DQ21	45	RAS1
10	Vcc	46	NC
11	NC	47	$\overline{W}$
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	Res(A10)	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	Vcc
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	Res(A11)	65	DQ16
30	Vcc	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	RAS3	69	PD3
34	RAS2	70	PD4
35	DQ26	71	NC
36	DQ8	72	Vss

### PRESENCE DETECT PINS (Optional)

Pin	60NS
PD1	NC
PD2	NC
PD3	NC
PD4	NC



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### ABSOLUTE MAXIMUM RATINGS \*

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V <sub>cc</sub>	-1 to +7.0	V
Storage Temperature	T <sub>stg</sub>	-55 to +150	°C
Power Dissipation	P <sub>d</sub>	6	W
Short Circuit Output Current	I <sub>OS</sub>	50	mA

\* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, Ta = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V <sub>cc</sub>	4.5	5.0	5.5	V
Ground	V <sub>ss</sub>	0	0	0	V
Input High Voltage	V <sub>IH</sub>	2.4	-	V <sub>cc</sub> +1*1	V
Input Low Voltage	V <sub>IL</sub>	-1.0*2	-	0.8	V

\*1: V<sub>cc</sub>+2.0V/20ns (5V), Pulse width is measured at V<sub>cc</sub>.

\*2: -2.0V/20ns (5V), Pulse width is measured at V<sub>ss</sub>.

### DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	AVED2M361JSQW-XX		Unit
		Min	Max	
ICC1	-60	-	381	mA
ICC2	-	-	12	mA
ICC3	-60	-	381	mA
ICC4	-60	-	281	mA
ICC5	-	-	6	mA
ICC6	-60	-	381	mA
I1(L)	-	-30	30	μA
IO(L)	-	-10	10	μA
VOH	-	2.4	-	V
VOL	-	-	0.4	V

ICC1: Operating Current \* [  $\overline{RAS}$ ,  $\overline{LCAS}$ ,  $\overline{UCAS}$  Address cycling @tRC=min.]

ICC2: Standby Current [  $\overline{RAS} = \overline{LCAS} = \overline{UCAS} = \overline{W} = V_{IH}$  ]

ICC3:  $\overline{RAS}$  Only Refresh Current \* [  $\overline{LCAS} = \overline{UCAS} = V_{IH}$ ,  $\overline{RAS}$ , Address cycling @tRC = min.]

ICC4: Fast Page Mode Current \* [  $\overline{RAS} = \overline{VIL}$ ,  $\overline{LCAS}$  or  $\overline{UCAS}$ , Address cycling @ tPC=min.]

ICC5: Standby Current [  $\overline{RAS} = \overline{LCAS} = \overline{UCAS} = \overline{W} = V_{cc}-0.2V$  ]

ICC6:  $\overline{CAS}$ -Before- $\overline{RAS}$  Refresh Current \* [  $\overline{RAS}$  and  $\overline{CAS}$  cycling @ tRC = min.]

I1(L): Input Leakage Current (Any input  $0 \leq V_{IN} \leq V_{cc}+0.5V$ , all other pins not under test = 0 V.)

IO(L): Output Leakage Current (Data out is disabled,  $0V \leq V_{out} \leq V_{cc}$ )

VOH: Output High Voltage Level (IOH = -5mA)

VOL: Output Low Voltage Level (IOL = 4.2mA)

\* NOTE: ICC1, ICC3, ICC4 and ICC6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. ICC is specified as an average current. In ICC1 and ICC3, address can be changed maximum once while  $\overline{RAS} = \overline{VIL}$ . In ICC4, address can be changed maximum once within one FPM page mode cycle, tPC.



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**CAPACITANCE** [Ta = 25 °C, f=1MHz]

Item	Symbol	Min	Max	Unit
Input capacitance [AO - A9]	CIN1	-	50	pF
Input capacitance [ $\overline{W}$ ]	CIN2	-	60	pF
Input capacitance [ $\overline{RAS0}$ , RAS3 ]	CIN3	-	30	pF
Input capacitance [ $\overline{CAS0}$ - $\overline{CAS3}$ ]	CIN4	-	40	pF
Input/Output capacitance [DQ0-35]	CDQ	-	30	pF

**AC CHARACTERISTICS** [0°C ≤ Ta ≤ 70°C, Vcc=5.0V ±10%. See notes 1,2.]

STANDARD OPERATION	Symbol	-60		Unit	Notes
		Min	Max		
Random read or write cycle time	tRC	110	-	ns	
Access time from $\overline{RAS}$	tRAC	-	60	ns	3,4,10
Access time from $\overline{CAS}$	tCAC	-	17	ns	3,4,5
Access time from column address	tAA	-	30	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	3	0	ns	3
Output buffer turn-off delay	tCEZ	3	15	ns	6,11,12
Transition time [rise and fall]	tT	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	40	-	ns	
$\overline{RAS}$ pulse width	tRAS	60	10K	ns	
$\overline{RAS}$ hold time	tRSH	17	-	ns	
$\overline{CAS}$ hold time	tCSH	50	-	ns	
$\overline{CAS}$ pulse width	tCAS	10	10K	ns	13
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	45	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	30	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5	-	ns	
Row address set-up time	tASR	0	0	ns	
Row address hold time	tRAH	10	-	ns	
Column address set-up time	tASC	0	0	ns	
Column address hold time	tCAH	10	-	ns	
Column address to $\overline{RAS}$ lead time	tRAL	30	-	ns	
Read command set-up time	tRCS	0	0	ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0	0	ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0	0	ns	8
Write command hold time	tWCH	10	-	ns	
Write command pulse width	tWP	10	-	ns	



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**AC CHARACTERISITICS** (continued)

STANDARD OPERATION	Symbol	-60		Unit	Notes
		Min	Max		
Write command to $\overline{\text{RAS}}$ lead time	tRWL	15	-	ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	10	-	ns	
Data set-up time	tDS	0	0	ns	9
Data hold time	tDH	10	-	ns	9
Refresh period (2K)	tREF	-	16	ms	
Write command set-up time	tWCS	0	0	ns	7
CAS set-up time [CAS - before - RAS refresh]	tCSR	5	-	ns	
$\overline{\text{CAS}}$ hold time [CAS - before - RAS refresh]	tCHR	10	-	ns	
RAS precharge to CAS hold time	tRPC	5	-	ns	
$\overline{\text{CAS}}$ precharge time ( $\overline{\text{C-B-R}}$ test cycle)	tCPT	20	-	ns	
Access time from $\overline{\text{CAS}}$ precharge	tCPA	-	35	ns	3
Fast Page mode cycle time	tHPC	30	-	ns	13
$\overline{\text{CAS}}$ precharge time (Hyper Page cycle)	tCP	10	-	ns	
RAS pulse width (Hyper Page cycle)	tRASP	60	200K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	tRHCP	35	-	ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ precharge time ( $\overline{\text{C-B-R}}$ refresh)	tWRP	10	-	ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ hold time ( $\overline{\text{C-B-R}}$ refresh)	tWRH	10	-	ns	
Output data hold time	tDOH	5	-	ns	
Output buffer turn off delay from $\overline{\text{RAS}}$	tREZ	3	15	ns	6,11,12
Output buffer turn off delay from $\overline{\text{W}}$	tWEZ	3	15	ns	6,11
$\overline{\text{W}}$ to data delay	tWED	15	-	ns	
$\overline{\text{W}}$ pulse width (Hyper Page Cycle)	tWPE	5	-	ns	
Hold time $\overline{\text{CAS}}$ low to $\overline{\text{CAS}}$ high	tCLCH	5	-	ns	



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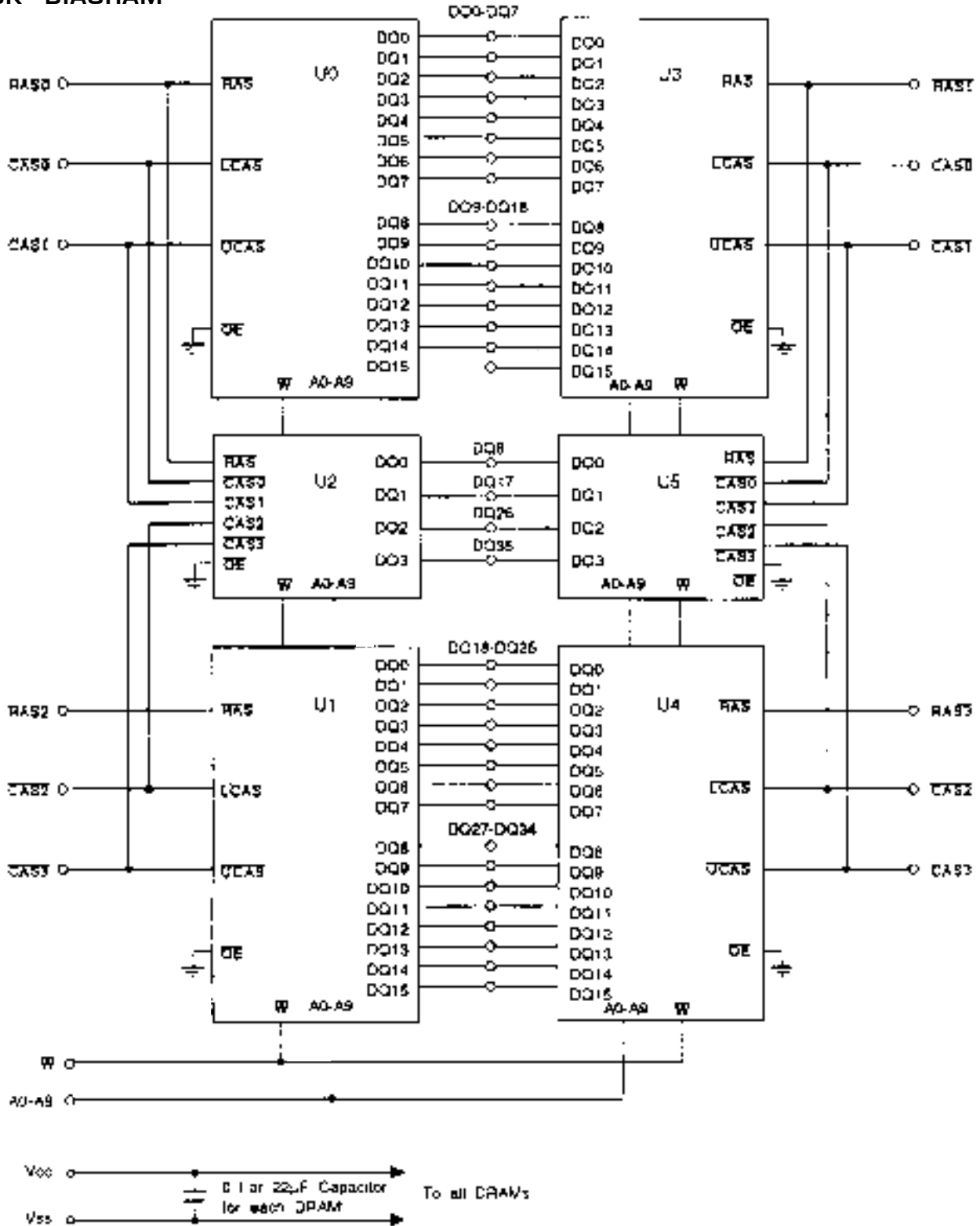
NOTES

1. An initial pause of 200 $\mu$ s is required after power-up followed by any 8  $\overline{\text{RAS}}$  -only or  $\overline{\text{CAS}}$  -before-  $\overline{\text{RAS}}$  refresh cycles before proper device operation is achieved.
2.  $V_{IH}$  (min) and  $V_{IL}$  (max) are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}$  (min) and  $V_{IL}$  (max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2TTL loads and 100pF.
4. Operation within the  $t_{RCD}$  (max) limit insures that  $t_{RAC}$  (max) can be met.  $t_{RCD}$  (max) is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (max) limit, then access time is controlled exclusively by  $t_{CAC}$ .
5. Assumes that  $t_{RCD} \geq t_{RCD}$  (max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to  $V_{OH}$  or  $V_{OL}$ .
7.  $t_{WCS}$  is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}$  (min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
8. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
9. These parameters are referenced to the  $\overline{\text{CAS}}$  leading edge in early write cycles and to the  $\overline{W}$  leading edge in read-write cycles.
10. Operation within the  $t_{RAD}$  (max) limit insures that  $t_{RAC}$  (max) can be met.  $t_{RAD}$  (max) is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}$  (max) limit, then access time is controlled by  $t_{AA}$ .
11.  $t_{CEZ}$ (max),  $t_{REZ}$ (max),  $t_{WEZ}$ (max) and  $t_{OEZ}$ (max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
12. If  $\overline{\text{RAS}}$  goes high before  $\overline{\text{CAS}}$  goes high, the open circuit condition of the output is achieved by  $\overline{\text{CAS}}$  going high. If  $\overline{\text{CAS}}$  goes high before  $\overline{\text{RAS}}$  goes high, the open circuit condition of the output is achieved by  $\overline{\text{RAS}}$  going high.
13.  $t_{ASC} \geq t_{CP}$ (min).
14. In order to hold the adress latched by the first  $\overline{\text{CAS}}$  going low, the parameter  $t_{CLCH}$  must be met.



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BLOCK DIAGRAM





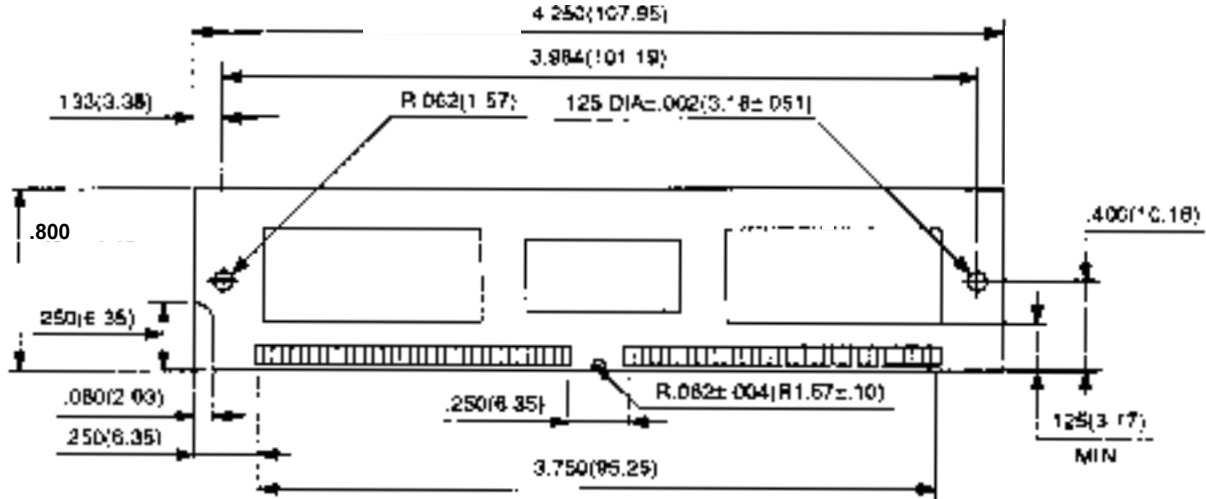
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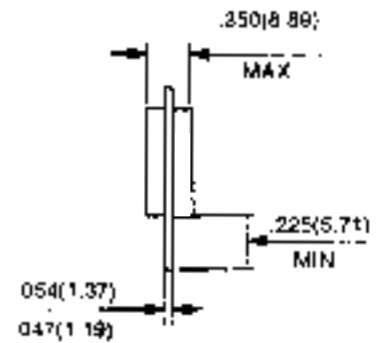
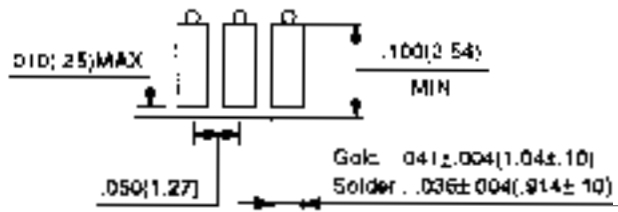
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PACKAGE DIMENSION



Gold & Solder Plating Lead



Tolerances: ± .005(.13) unless otherwise specified

Aved Memory Products reserves the right to change products and specifications without notice