



AVED MEMORY PRODUCTS

Where Quality & Memory Merge

AVED1M321KSMW-XX

FAST PAGE MODE 1M X 32 DRAM SIMM, 1K REFRESH, 5V

DESCRIPTION

AVED Memory Products AVED1M321KSMW-XX is a 1M bit x 32 Dynamic RAM high density memory module. The AVED Memory Products AVED1M321KSMW-XX consists of two CMOS 1Mx16bit DRAMs in 42-pin SOJ packages mounted on a 72-pin glass-epoxy substrate. A 0.22uf decoupling capacitor is mounted on the printed circuit board for each DRAM. The AVED Memory Products AVED1M321KSMW-XX is a Single In-Line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

APPLICATION

Main Memory unit for computer, Microcomputer memory, Refresh memory for CRT.

FEATURES

- Performance Ranges

Speed	tRAC	tCAC	tRC
-60	60ns	15ns	110ns
-70	70ns	20ns	130ns

- Part Identification
 - AVED1M321KSMW-XX
 - 1024 cycles/16ms Ref, SOJ, Gold Contact Plating
 - (XX= -60, -70)
- Fast Page Mode Operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single +5V \pm 10% power supply

PIN NAMES

A0 - A9	Address Inputs
DQ0 - DQ31	Data In/Out
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{RAS0}}$ $\overline{\text{RAS2}}$	Row Address Strobe
$\overline{\text{CAS0}}$ $\overline{\text{CAS3}}$	Column Address Strobe
PD1 - PD4	Presence Detect
Vcc	Power (+5V)
Vss	Ground
NC	No Connection
Res	Reserved Pin

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	Vss	37	NC
2	DQ0	38	NC
3	DQ16	39	Vss
4	DQ1	40	$\overline{\text{CAS0}}$
5	DQ17	41	$\overline{\text{CAS2}}$
6	DQ2	42	$\overline{\text{CAS3}}$
7	DQ18	43	$\overline{\text{CAS1}}$
8	DQ3	44	$\overline{\text{RAS0}}$
9	DQ19	45	Res($\overline{\text{RAS1}}$)
10	Vcc	46	NC
11	NC	47	$\overline{\text{W}}$
12	A0	48	NC
13	A1	49	DQ8
14	A2	50	DQ24
15	A3	51	DQ9
16	A4	52	DQ25
17	A5	53	DQ10
18	A6	54	DQ26
19	Res (A10)	55	DQ11
20	DQ4	56	DQ27
PD1	Vss	57	Vss
PD2	Vss	58	Vss
PD3	NC	59	Vcc
PD4	NC	60	NC
21	DQ20	61	DQ13
22	DQ5	62	DQ30
23	DQ21	63	DQ14
24	DQ6	64	DQ31
25	DQ22	65	DQ15
26	DQ7	66	NC
27	DQ23	67	PD1
28	A7	68	PD2
29	Res(A11)	69	PD3
30	Vcc	70	PD4
31	A8	71	NC
32	A9	72	Vss
33	Res($\overline{\text{RAS3}}$)		
34	$\overline{\text{RAS2}}$		
35	NC		
36	NC		

PRESENCE DETECT PINS (Optional)



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ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	Vcc	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	Pd	2	W
Short Circuit Output Current	IOS	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, Ta = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	VIH	2.4	-	Vcc+1**	V
Input Low Voltage	VIL	-1.0 ²	-	0.8	V

*1: Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc.

*2: -2.0V/20ns(5V), Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	AVED1M321KSMW-XX		Unit
		Min	Max	
ICC1	-60	-	320	mA
	-70	-	300	mA
ICC2	-	-	4	mA
ICC3	-60	-	320	mA
	-70	-	300	mA
ICC4	-60	-	220	mA
	-70	-	200	mA
ICC5	-	-	2	mA
ICC6	-60	-	320	mA
	-70	-	300	mA
I1(L)	-	-10	10	µA
I0(L)	-	-5	5	µA
VOH	-	2.4	-	V
VOL	-	-	0.4	V

ICC1: Operating Current * (\overline{RAS} , \overline{LCAS} or \overline{UCAS} Address cycling @tRC=min.)

ICC2: Standby Current ($\overline{RAS} = \overline{LCAS} = \overline{UCAS} = \overline{W} = V_{IH}$)

ICC3: \overline{RAS} Only Refresh Current * ($\overline{LCAS} = \overline{UCAS} = V_{IH}$, \overline{RAS} cycling @tRC = min.)

ICC4: Fast Page Mode Current * ($\overline{RAS} = V_{IL}$, \overline{LCAS} or \overline{UCAS} cycling : tPC=min.)

ICC5: Standby Current ($\overline{RAS} = \overline{LCAS} = \overline{UCAS} = \overline{W} = V_{cc}-0.2V$)

ICC6: \overline{CAS} -Before- \overline{RAS} Refresh Current * (\overline{RAS} and \overline{CAS} cycling @ tRC = min.)

I1(L): Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{cc}+0.5V$, all other pins not under test = 0 V.)

I0(L): Output Leakage Current (Data out is disabled, $0V \leq V_{out} \leq V_{cc}$)

VOH: Output High Voltage Level (IOH = -5mA)

VOL: Output Low Voltage Level (IOL = 4.2mA)

* NOTE: ICC1, ICC3, ICC4 and ICC6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. ICC is specified as an average current. In ICC1 and ICC3, address can be changed maximum two times while $\overline{RAS} = V_{IL}$. In ICC4, address can be changed maximum once within one page mode cycle.



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CAPACITANCE (Ta = 25 °C, Vcc=5V, f=1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance [A0-A9]	CIN1	-	30	pF
Input capacitance [\overline{W}]	CIN2	-	30	pF
Input capacitance [$\overline{RAS0}, \overline{RAS2}$]	CIN3	-	20	pF
Input capacitance [$\overline{CAS0} - \overline{CAS3}$]	CIN4	-	20	pF
Input/Output capacitance [DQ0-31]	CDQ	-	20	pF

AC CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, Vcc=5.0V ±10%. See notes 1,2.)

STANDARD OPERATION	Symbol	-60		-70		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	tRC	110		130		ns	
Access time from \overline{RAS}	tRAC		60		70	ns	3,4
Access time from \overline{CAS}	tCAC		15		20	ns	3,4,5
Access time from column address	tAA		30		35	ns	3,10
\overline{CAS} to output in Low-Z	tCLZ	0		0		ns	3
Output buffer turn-off delay	tOFF	0	15	0	15	ns	6
Transition time (rise and fall)	tT	3	50	3	50	ns	2
\overline{RAS} precharge time	tRP	40		50		ns	
\overline{RAS} pulse width	tRAS	60	10K	70	10K	ns	
\overline{RAS} hold time	tRSH	15		20		ns	
\overline{CAS} hold time	tCSH	60		70		ns	
\overline{CAS} pulse width	tCAS	15	10K	20	10K	ns	
\overline{RAS} to \overline{CAS} delay time	tRCD	20	45	20	50	ns	4
\overline{RAS} to column address delay time	tRAD	15	30	15	35	ns	10
\overline{CAS} to \overline{RAS} precharge time	tCRP	5		5		ns	
Row address set-up time	tASR	0		0		ns	
Row address hold time	tRAH	10		10		ns	
Column address set-up time	tASC	0		0		ns	
Column address hold time	tCAH	10		15		ns	
Column address to \overline{RAS} lead time	tRAL	30		35		ns	
Read command set-up time	tRCS	0		0		ns	
Read command hold time referenced to \overline{CAS}	tRCH	0		0		ns	8
Read command hold time referenced to \overline{RAS}	tRRH	0		0		ns	8
Write command hold time	tWCH	10		15		ns	
Write command pulse width	tWP	10		15		ns	
Write command to \overline{RAS} lead time	tRWL	15		15		ns	
Write command to \overline{CAS} lead time	tCWL	15		15		ns	
Data set-up time	tDS	0		0		ns	9



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AC CHARACTERISITICS (continued)

STANDARD OPERATION	Symbol	-60		-70		Unit	Notes
		Min	Max	Min	Max		
Data hold time	t _{DH}	10		15		ns	9
Refresh period	t _{REF}		16		16	ms	
Write command set-up time	t _{WCS}	0		0		ns	7
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ - before - $\overline{\text{RAS}}$ refresh)	t _{CSR}	5		5		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ - before - $\overline{\text{RAS}}$ refresh)	t _{CHR}	10		10		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	t _{RPC}	5		5		ns	
Access time from $\overline{\text{CAS}}$ precharge	t _{CPA}		35		40	ns	3
Fast Page cycle time	t _{PC}	40		45		ns	
$\overline{\text{CAS}}$ precharge time (Fast Page cycle)	t _{CP}	10		10		ns	
$\overline{\text{RAS}}$ pulse width (Fast Page cycle)	t _{RASP}	60	200K	70	200K	ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ precharge time ($\overline{\text{C}}$ -B- $\overline{\text{R}}$ refresh)	t _{WRP}	10		10		ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ hold time ($\overline{\text{C}}$ -B- $\overline{\text{R}}$ refresh)	t _{WRH}	10		10		ns	
$\overline{\text{CAS}}$ precharge time ($\overline{\text{C}}$ -B- $\overline{\text{R}}$ counter test cycle)	t _{CPT}	20		25		ns	



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NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles before proper device operation is achieved.
2. VIH (min) and VIL (max) are reference levels for measuring timing of input signals. Transition times are measured between VIH (min) and VIL (max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2TTL loads and 100pF.
4. Operation within the tRCD (max) limit insures that tRAC (max) can be met. tRCD (max) is specified as a reference point only. If tRCD is greater than the specified tRCD (max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD \geq tRCD (max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
7. tWCS is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If tWCS \geq tWCS (min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles.
10. Operation within the tRAD (max) limit insures that tRAC (max) can be met. tRAD (max) is specified as a reference point only. If tRAD is greater than the specified tRAD (max) limit, then access time is controlled by tAA.



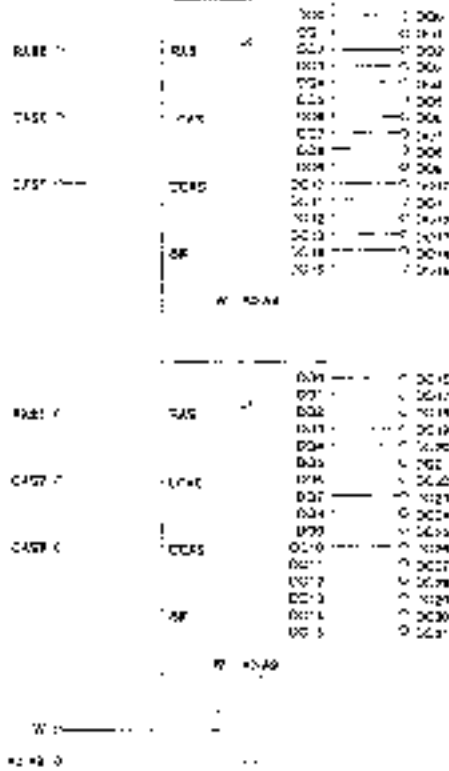
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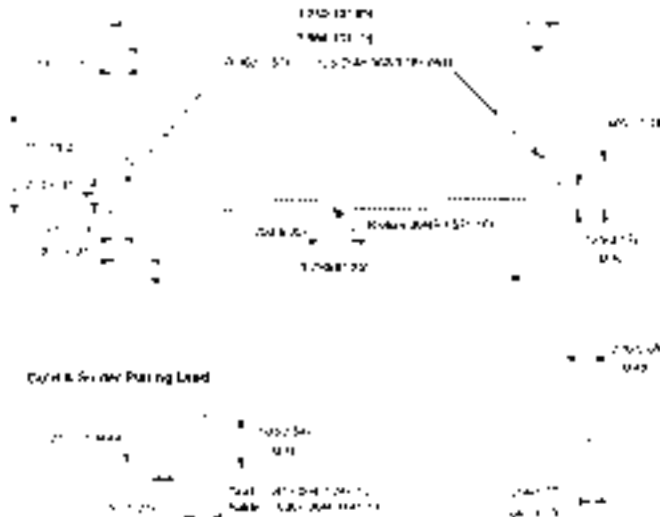
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FUNCTIONAL BLOCK DIAGRAM



To all DRAMs

PACKAGE DIMENSIONS



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