



AVED MEMORY PRODUCTS

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AVED4F664LSD16-XX

FAST PAGE MODE with EDO 4M X 64 DRAM DIMM, LOW POWER, without BUFFER, 4K REFRESH, 3.3V

DESCRIPTION

AVED Memory Products AVED4F664LSD16-XX is a 4M bit X 64 Dynamic RAM high density memory module. The AVED Memory Products AVED4F664LSD16-XX consists of four CMOS 4M X 16bit DRAMs in 50-pin TSOP 400mil packages and a 1K or 2K EEPROM in 8-pin SOP package mounted on a 144-pin glass-epoxy substrate. A 0.22uf decoupling capacitor is mounted on the printed circuit board for each DRAM. The AVED Memory Products AVED4F664LSD16-XX is a Small Outline Dual In-Line Memory Module and is intended for mounting into 144-pin edge connector sockets.

APPLICATION

Main Memory unit for computer, Microcomputer memory, Refresh memory for CRT.

FEATURES

• Performance Ranges

Speed	tRAC	tCAC	tRC	tHPC
-50	50ns	13ns	90ns	25ns
-60	60ns	15ns	110ns	30ns

- Part Identification
 - AVED4F664LSD16-XX
 - 4096 cycles/128ms Ref, TSOP, Gold Contact Plating
 - (XL = -50, -60)
- EDO Mode Operation
- Serial Presence Detect with EEPROM
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single +3.3V \pm 0.3V power supply
- Self-Refresh capability

PIN NAMES

Pin Name	Function
A0 - A11	Address Input (4K Ref)
DQ0 - DQ63	Data In/Out
$\overline{\text{W}}$	Read/Write Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{RAS0}}$	Row Address Strobe
$\overline{\text{CAS0}} - \overline{\text{CAS7}}$	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
SDA	Serial Address/Data I/O
SCL	Serial Clock
RSVD	Reserved Use
RFU	Reserved For Future Use



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PIN CONFIGURATIONS (FRONT SIDE/BACK SIDE)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	49	DQ13	50	DQ45	97	DQ22	98	DQ54
3	DQ0	4	DQ32	51	DQ14	52	DQ46	99	DQ23	100	DQ55
5	DQ1	6	DQ33	53	DQ15	54	DQ47	101	Vcc	102	Vcc
7	DQ2	8	DQ34	55	Vss	56	Vss	103	A6	104	A7
9	DQ3	10	DQ35	57	RSVD	58	RSVD	105	A8	106	A11
11	Vcc	12	Vcc	59	RSVD	60	RSVD	107	Vss	108	Vss
13	DQ4	14	DQ36	61	RFU	62	RFU	109	A9	110	NC
15	DQ5	16	DQ37	63	Vcc	64	Vcc	111	A10	112	NC
17	DQ6	18	DQ38	65	RFU	66	RFU	113	Vcc	114	Vcc
19	DQ7	20	DQ39	67	\bar{w}	68	RFU	115	$\bar{CAS}2$	116	$\bar{CAS}6$
21	Vss	22	Vss	69	$\bar{RAS}0$	70	RFU	117	$\bar{CAS}3$	118	$\bar{CAS}7$
23	$\bar{CAS}0$	24	$\bar{CAS}4$	71	NC	72	RFU	119	Vss	120	Vss
25	$\bar{CAS}1$	26	$\bar{CAS}5$	73	\bar{OE}	74	RFU	121	DQ24	122	DQ56
27	Vcc	28	Vcc	75	Vss	76	Vss	123	DQ25	124	DQ57
29	A0	30	A3	77	RSVD	78	RSVD	125	DQ26	126	DQ58
31	A1	32	A4	79	RSVD	80	RSVD	127	DQ27	128	DQ59
33	A2	34	A5	81	Vcc	82	Vcc	129	Vcc	130	Vcc
35	Vss	36	Vss	83	DQ16	84	DQ48	131	DQ28	132	DQ60
37	DQ8	38	DQ40	85	DQ17	86	DQ49	133	DQ29	134	DQ61
39	DQ9	40	DQ41	87	DQ18	88	DQ50	135	DQ30	136	DQ62
41	DQ10	42	DQ42	89	DQ19	90	DQ51	137	DQ31	138	DQ63
43	DQ11	44	DQ43	91	Vss	92	Vss	139	Vss	140	Vss
45	Vcc	46	Vcc	93	DQ20	94	DQ52	141	SDA	142	SCL
47	DQ12	48	DQ44	95	DQ21	96	DQ53	143	Vcc	144	Vcc

Note: A11 is used for only AVED2F664LSD8 (4K Ref.)



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SERIAL PRESENCE DETECT INFORMATION

- Serial PD Interface Protocol: IIC
- Current sink capability of SDA driver $\leq 3\text{mA}$
- Maximum clock frequency: 80KHz
- Contents:

Byte Number	Function Described	Function Supported	Hex Value
0	Number of bytes used by Module Manufacturer	13bytes	0Dh
1	Total SPD memory size	128bytes (1K-bit)	07h
		256bytes (2K-bit)	08h
2	Memory type	EDO	02h
3	Number of ROW Addresses	12 (4K Ref)	0Ch
4	Number of COLUMN Addresses	10 (4K Ref)	0Ah
5	Number of Banks	1	01h
6	Module Data Width	64bits	40h
7	Module Data Width (Continued)	not used	00h
8	Module Interface Levels	LVTTL	01h
9	RAS Access Time (tRAC)	50ns (-5)	32h
		60ns (-6)	3Ch
10	CAS Access Time (tCAC)	13ns (-5)	0Dh
		15ns (-6)	0Fh
11	Module Configuration Type	None	00h
12	Refresh Rate/Type	Extended(2x) --31.3 μs	83h
13~	Undefined	Undefined	Undefined

Above data are based on the SPD specification of JEDEC standard.



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ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	VIN, VOUT	-0.5 to +4.6	V
Voltage on Vcc supply relative to Vss	Vdd	-0.5 to +4.6	V
Storage Temperature	Tstg	-55 to +125	°C
Power Dissipation	Pd	4	W
Short Circuit Output Current	IOS	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, Ta = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vdd	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input High Voltage	VIH	2.0	-	Vdd + 0.3 *1	V
Input Low Voltage	VIL	-0.3 *2	-	0.8	V

*1: Vdd+1.3V at Pulse width ≤ 15ns, which is measured at Vdd.

*2: -1.3V at Pulse width ≤ 15ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	AVED4F664LSD16-XX		Unit
		Min	Max	
ICC1	-50	-	600	mA
	-60	-	560	mA
ICC2	-	-	4	mA
ICC3	-50	-	600	mA
	-60	-	560	mA
ICC4	-50	-	480	mA
	-60	-	440	mA
ICC5	-	-	1.2	mA
ICC6	-50	-	600	mA
	-60	-	560	mA
ICC7	-	-	2.2	mA
ICCS	-	-	1.8	mA
I1(L)	-	-20	20	µA
I0(L)	-	-5	5	µA
VOH	-	2.4	-	V
VOL	-	-	0.4	V

- ICC1: Operating Current * (\overline{RAS} , \overline{CAS} , Address cycling @tRC=min.)
- ICC2: Standby Current ($RAS = CAS = W = VIH$)
- ICC3: RAS Only Refresh Current * ($CAS = VIH$, RAS cycling @tRC = min.)
- ICC4: Fast Page Mode Current * ($\overline{RAS} = VIL$, \overline{CAS} cycling : tPC=min.)
- ICC5: Standby Current ($RAS = CAS = W = Vcc-0.2V$)
- ICC6: \overline{CAS} -Before- \overline{RAS} Refresh Current * (RAS and \overline{CAS} cycling @ tRC = min.)
- ICC7: Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage (VIH)=Vcc-0.2V, Input low voltage (VIL)=0.2V, \overline{UCAS} , $\overline{LCAS} = 0.2V$,
Din = Don't Care, tRC = 31.25µs (4K/L-ver), 62.5µs (2K/L-ver), tRAS = tRAS min ~300ns
- ICCS: Self Refresh Current
 $RAS = \overline{UCAS} = \overline{LCAS} = VIL$, $\overline{W} = \overline{OE} = A0 - A11 = Vcc-0.2V$ or 0.2V
DQ0 ~ DQ63 = Vcc-0.2V, 0.2V or Open
- I1(L): Input Leakage Current (Any input $0 \leq VIN \leq Vcc+0.3V$, all other pins not under test = 0 V.)
- I0(L): Output Leakage Current (Data out is disabled, $0V \leq Vout \leq Vcc$)
- VOH: Output High Voltage Level (IOH = -2mA)
- VOL: Output Low Voltage Level (IOL =2mA)

* NOTE: ICC1, ICC3, ICC4 and ICC6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. ICC is specified as an average current. In ICC1 and ICC3, address can be changed maximum once while $RAS = VIL$. In ICC4, address can be changed maximum once within one page mode cycle.



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CAPACITANCE (Ta = 25 °C, Vcc=3.3V, f=1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance [A0-A11]	CIN1	-	30	pF
Input capacitance [\overline{W} , \overline{OE}]	CIN2	-	38	pF
Input capacitance [$\overline{RAS0}$]	CIN3	-	38	pF
Input capacitance [$\overline{CAS0}$ - $\overline{CAS7}$]	CIN4	-	17	pF
Input/Output capacitance [DQ0 - 63]	CDQ1	-	17	pF

AC CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, See notes 1,2.)

Test Condition: Vcc=3.3V±0.3V, Vih/Vil=2.0/0.8V, Voh/Vol=2.0/0.8V.

STANDARD OPERATION	Symbol	-50		-60		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		ns	
Read-modify-write cycle time	tRWC	131		155		ns	
Access time from \overline{RAS}	tRAC		50		60	ns	
Access time from \overline{CAS}	tCAC		13		15	ns	3,4,5
Access time from column address	tAA		25		30	ns	3,9
\overline{CAS} to output in Low-Z	tCLZ	3		3		ns	3
\overline{OE} to output in Low-Z	tOLZ	3		3		ns	3
Output buffer turn-off delay from \overline{CAS}	tCEZ	3	13	3	13	ns	3,12
Transition time (rise and fall)	tT	2	50	2	50	ns	2
\overline{RAS} precharge time	tRP	30		40		ns	
\overline{RAS} pulse width	tRAS	50	10K	60	10K	ns	
\overline{RAS} hold time	tRSH	13		15		ns	
\overline{CAS} hold time	tCSH	38		45		ns	
\overline{CAS} pulse width	tCAS	8	10K	10	10K	ns	
\overline{RAS} to \overline{CAS} delay time	tRCD	20	37	20	45	ns	4
\overline{RAS} to column address delay time	tRAD	15	25	15	30	ns	9
\overline{CAS} to \overline{RAS} precharge time	tCRP	5		5		ns	
Row address set-up time	tASR	0		0		ns	
Row address hold time	tRAH	10		10		ns	
Column address set-up time	tASC	0		0		ns	
Column address hold time	tCAH	8		10		ns	
Column address to \overline{RAS} lead time	tRAL	25		30		ns	
Read command set-up time	tRCS	0		0		ns	
Read command hold time referenced to \overline{CAS}	tRCH	0		0		ns	7
Read command hold time referenced to \overline{RAS}	tRRH	0		0		ns	7
Write command set-up time	tWCS	0		0		ns	6
Write command hold time	tWCH	10		10		ns	6
Write command pulse width	tWP	10		10		ns	
Write command to \overline{RAS} lead time	tRWL	13		15		ns	



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AC CHARACTERISTICS (continued)

STANDARD OPERATION	Symbol	-50		-60		Unit	Notes
		Min	Max	Min	Max		
Write command to $\overline{\text{CAS}}$ lead time	tCWL	8		10		ns	
Data set-up time	tDS	0		0		ns	8
Data hold time	tDH	8		10		ns	8
Refresh period (L-ver)	tREF		128		128	ms	
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tCWD	36		38		ns	6
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	tRWD	73		83		ns	6
Column address to $\overline{\text{W}}$ delay time	tAWD	48		53		ns	6
$\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time	tCPWD	53		60		ns	6
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ - before - $\overline{\text{RAS}}$ refresh)	tCSR	10		10		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ - before - $\overline{\text{RAS}}$ refresh)	tCHR	10		10		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	tRPC	5		5		ns	
$\overline{\text{CAS}}$ precharge time ($\overline{\text{C}}$ -B- $\overline{\text{R}}$ counter test cycle)	tCPT	20		20		ns	
Access time from $\overline{\text{CAS}}$ precharge	tCPA		28		35	ns	3
Hyper Page mode cycle time	tHPC	25		30		ns	10
Hyper Page mode read-modify-write cycle time	tHPRWC	67		73		ns	10
$\overline{\text{CAS}}$ precharge time (Hyper Page cycle)	tCP	8		10		ns	13
$\overline{\text{RAS}}$ pulse width (Hyper Page cycle)	tRASP	50	200K	60	200K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	tRHCP	30		35		ns	
$\overline{\text{OE}}$ access time	tOEA		13		15	ns	3
$\overline{\text{OE}}$ to data delay	tOED	13		13		ns	
Output buffer turn off delay time from $\overline{\text{OE}}$	tOEZ	3	13	3	13	ns	
$\overline{\text{OE}}$ command hold time	tOEH	13		15		ns	
Output data hold time	tDOH	5		5		ns	
Output buffer turn off delay from $\overline{\text{RAS}}$	tREZ	3	13	3	15	ns	12
Output buffer turn off delay from $\overline{\text{W}}$	tWEZ	3	13	3	15	ns	
$\overline{\text{W}}$ to data delay	tWED	15		15		ns	
$\overline{\text{OE}}$ to $\overline{\text{CAS}}$ hold time	tOCH	5		5		ns	
$\overline{\text{CAS}}$ hold time to $\overline{\text{OE}}$	tCHO	5		5		ns	
$\overline{\text{OE}}$ precharge time	tOEP	5		5		ns	
$\overline{\text{W}}$ pulse width	tWPE	5		5		ns	
$\overline{\text{RAS}}$ pulse width ($\overline{\text{C}}$ -B- $\overline{\text{R}}$ self refresh)	tRASS	100		100		us	11
$\overline{\text{RAS}}$ precharge time ($\overline{\text{C}}$ -B- $\overline{\text{R}}$ self refresh)	tRPS	90		110		ns	11
$\overline{\text{CAS}}$ hold time ($\overline{\text{C}}$ -B- $\overline{\text{R}}$ self refresh)	tCHS	-50		-50		ns	11



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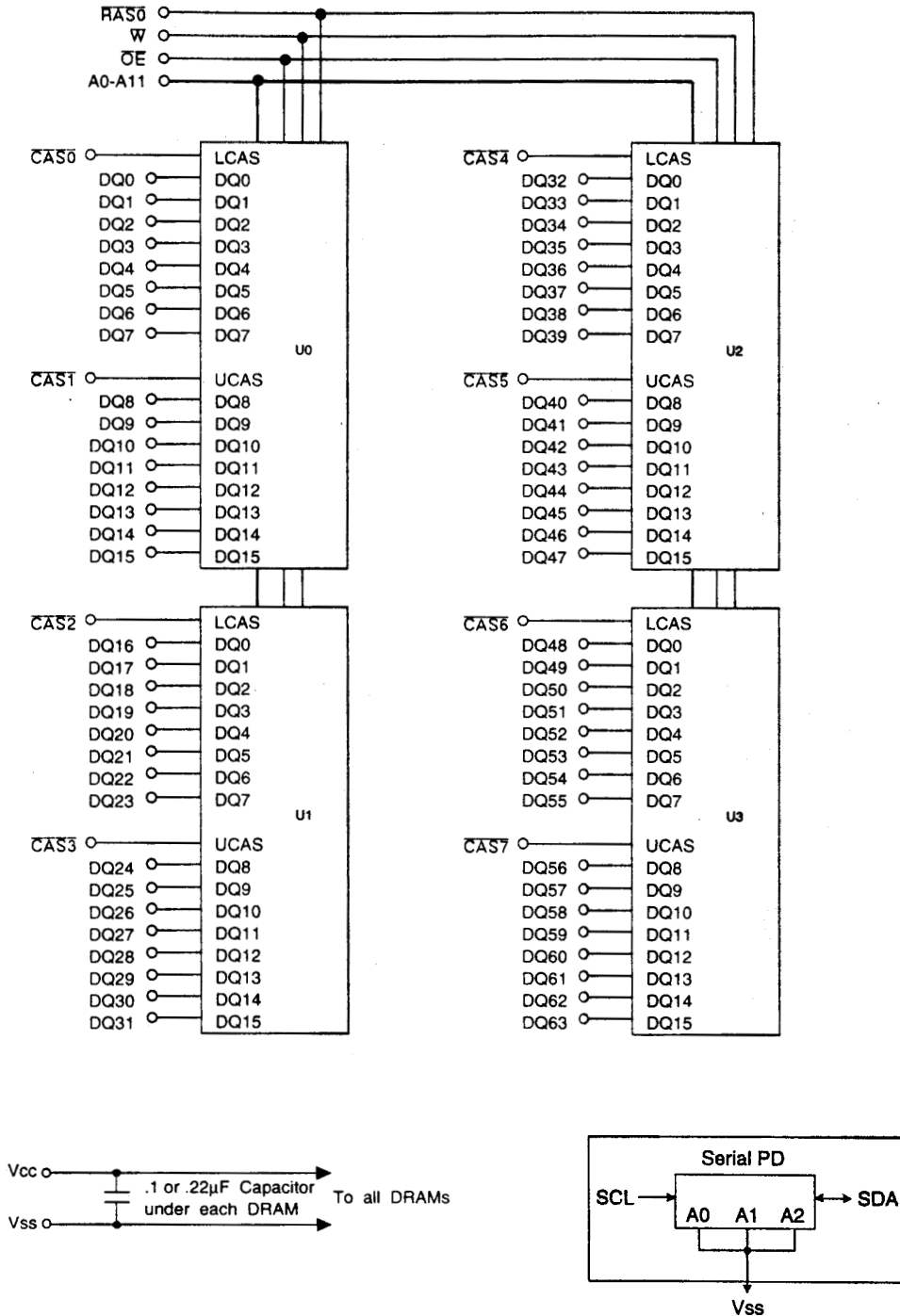
NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles before proper device operation is achieved.
2. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} (min) and V_{IL} (max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1TTL loads and 100pF.
4. Operation within the tCRD (max) limit insures that tRAC (max) can be met. tRCD (max) is specified as a reference point only. If tRCD is greater than the specified tRCD (max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD \geq tRCD (max).
6. tWCS is non restrictive operating parameter. It is included in the data sheet as electrical characteristic only. If tWCS \geq tWCS (min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
7. Either tRCH or tRRH must be satisfied for a read cycle.
8. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles.
9. Operation within the tRAD (max) limit insures that tRAC (max) can be met. tRAD (max) is specified as reference point only. If tRAD is greater than the specified tRAD (max) limit, then access time is controlled by tAA.
10. tASC \geq 6ns, Assume tT=2.0ns.
11. For all of the refresh mode except distributed $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh, 4096 cycle (2048 cycle) of burst refresh must be executed within 16ms before and after self-refresh in order to meet refresh specification.
12. If $\overline{\text{RAS}}$ goes high before $\overline{\text{CAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{CAS}}$ high going. If $\overline{\text{CAS}}$ goes high before $\overline{\text{RAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{RAS}}$ going.
13. tASC, tCAH are referenced to the earlier $\overline{\text{CAS}}$ falling edge.
14. tCP is specified from the last $\overline{\text{CAS}}$ rising edge in the previous cycle to the first $\overline{\text{CAS}}$ falling edge in the next cycle.
15. tCWD is referenced to the later $\overline{\text{CAS}}$ falling edge at word read-modify-write cycle.
16. tCWL is specified from $\overline{\text{W}}$ falling edge to the earlier $\overline{\text{CAS}}$ rising edge.
17. tCSR is referenced to earlier $\overline{\text{CAS}}$ falling low before $\overline{\text{RAS}}$ transition low.
18. tCSR is referenced to the later $\overline{\text{CAS}}$ rising after $\overline{\text{RAS}}$ transition low.
19. tDS, tDH is specified by the earlier $\overline{\text{CAS}}$ falling edge.



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FUNCTIONAL BLOCK DIAGRAM



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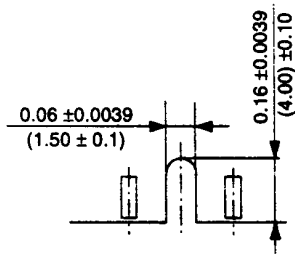
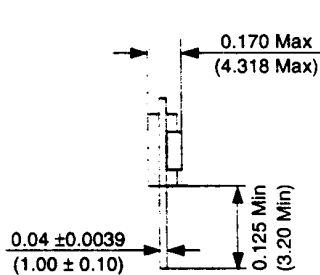
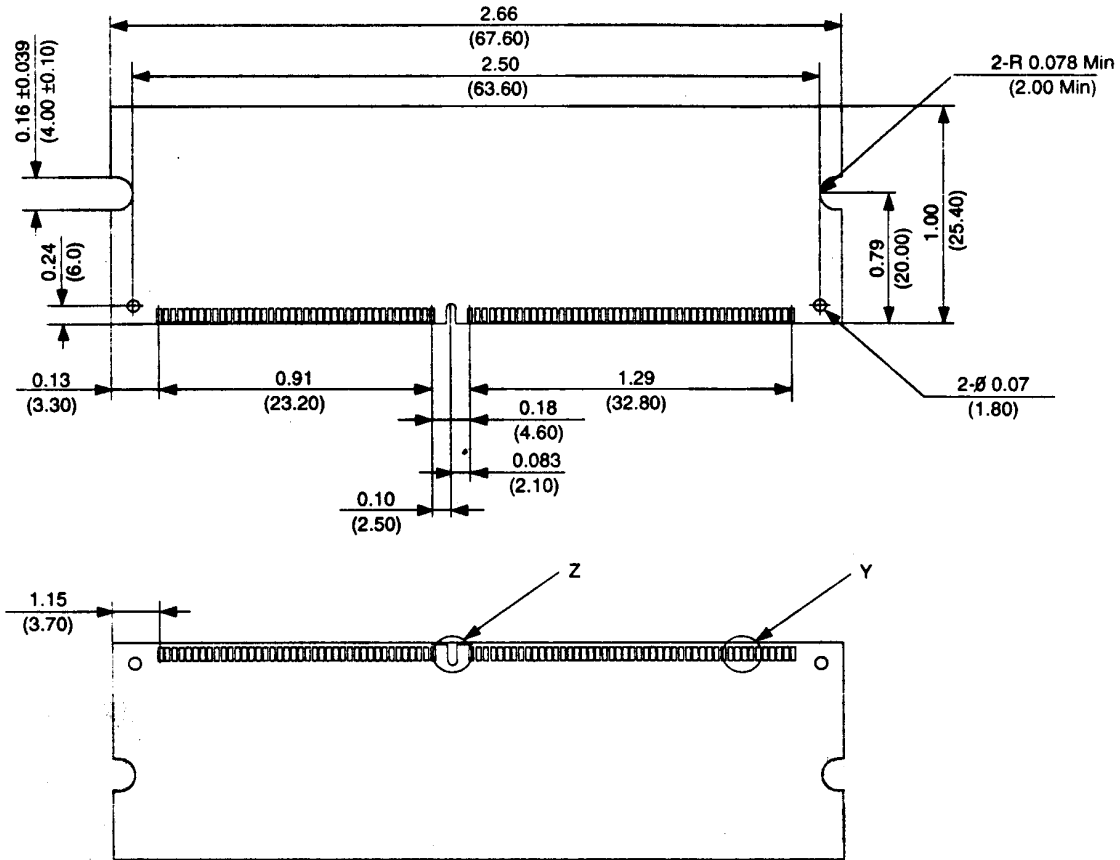
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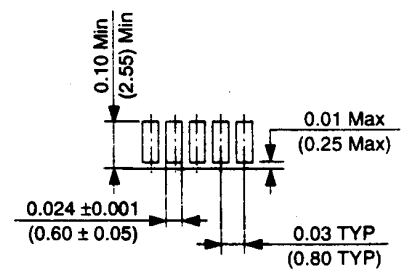
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PACKAGE DIMENSIONS

Units: Inches (millimeters)



Detail Z



Detail Y

Tolerances: ± .005 (.13) unless otherwise specified