



AVED MEMORY PRODUCTS

Where Quality & Memory Merge

AVED4M322SSM4/LSM4

FAST PAGE MODE 4MX32 DRAM SIMM, 2K REFRESH, 5V

DESCRIPTION

AVED Memory Products AVED4M322SSM4/LSM4 is a 4M bit x 32 Dynamic RAM high density memory module. The AVED Memory Products AVED4M322SSM4/LSM4 consists of eight CMOS 4Mx4bit DRAMs in 24-pin SOJ packages mounted on a 72-pin glass-epoxy substrate. A 0.22uf decoupling capacitor is mounted on the printed circuit board for each DRAM.

The AVED Memory Products AVED4M322SSM4/LSM4 is a Single In-Line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

APPLICATION

Main Memory unit for computer, Microcomputer memory, Refresh memory for CRT.

FEATURES

- Performance Ranges

Speed	tRAC	tCAC	tRC
-50	50ns	13ns	90ns
-60	60ns	15ns	110ns
-70	70ns	20ns	130ns

- Part Identification
 - AVED4M322SSM4-XX
2048 cycles/32ms Ref, SOJ, Tin Contact Plating
 - AVED4M322LSM4-XX
2048 cycles/32ms Ref, SOJ, Gold Contact Plating
 - XX= -50, -60, -70
- Fast Page Mode Operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single +5V \pm 10% power supply

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	Vss	37	NC
2	DQ0	38	NC
3	DQ16	39	Vss
4	DQ1	40	CAS0
5	DQ17	41	CAS2
6	DQ2	42	CAS3
7	DQ18	43	CAS1
8	DQ3	44	RAS0
9	DQ19	45	NC
10	Vcc	46	NC
11	NC	47	w
12	A0	48	NC
13	A1	49	DQ8
14	A2	50	DQ24
15	A3	51	DQ9
16	A4	52	DQ25
17	A5	53	DQ10
18	A6	54	DQ26
19	A10	55	DQ11
20	DQ4	56	DQ27
21	DQ20	57	DQ12
22	DQ5	58	$\overline{\text{DQ}}28$
23	DQ21	59	$\overline{\text{Vcc}}$
24	DQ6	60	$\overline{\text{DQ}}29$
25	DQ22	61	$\overline{\text{DQ}}13$
26	DQ7	62	$\overline{\text{DQ}}30$
27	DQ23	63	DQ14
28	A7	64	DQ31
29	NC	65	$\overline{\text{DQ}}15$
30	Vcc	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	NC	69	PD3

PIN NAMES

A0 - A10	Address Inputs
DQ0 - DQ31	Data In/Out
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{RAS}}0, \overline{\text{RAS}}2$	Row Address Strobe
$\overline{\text{CAS}}0, \overline{\text{CAS}}3$	Column Address Strobe
PD1 - PD4	Presence Detect
Vcc	Power (+5V)
Vss	Ground
NC	No Connection

PRESENCE DETECT PINS (Optional)

Pin	50NS	60NS	70NS
PD1	Vss	Vss	Vss
PD2	NC	NC	NC
PD3	Vss	NC	Vss
PD4	Vss	NC	NC



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ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	Vcc	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	Pd	8	W
Short Circuit Output Current	IOS	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, Ta = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V _{IH}	2.4	-	Vcc+1	V
Input Low Voltage	V _{IL}	-1.0	-	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	AVED4M322SSM4/LSM4		Unit
		Min	Max	
ICC1	-50	-	880	mA
	-60	-	800	mA
	-70	-	720	mA
ICC2	-	-	16	mA
ICC3	-50	-	880	mA
	-60	-	800	mA
	-70	-	720	mA
ICC4	-50	-	720	mA
	-60	-	640	mA
	-70	-	560	mA
ICC5	-	-	8	mA
ICC6	-50	-	880	mA
	-60	-	800	mA
	-70	-	720	mA
I1(L)	-	-80	80	µA
I0(L)	-	-10	10	µA
VOH	-	2.4	-	V
VOL	-	-	0.4	V

ICC1: Operating Current * (\overline{RAS} , \overline{CAS} , Address cycling @tRC=min.)

ICC2: Standby Current ($\overline{RAS} = \overline{CAS} = \overline{W} = V_{IH}$)

ICC3: \overline{RAS} Only Refresh Current * ($\overline{CAS} = V_{IH}$, \overline{RAS} cycling @tRC = min.)

ICC4: Average Power Supply current Fast Page Mode($\overline{RAS} = V_{IL}$, \overline{CAS} cycling, tPC=min.)

ICC5: Standby Current ($\overline{RAS} = \overline{CAS} = \overline{W} = V_{cc}-0.2V$)

ICC6: \overline{CAS} -Before- \overline{RAS} Refresh Current * (\overline{RAS} before- \overline{CAS} cycling, @ tRC = min.)

I1(L): Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{cc}+0.5V$, all other pins not under test = 0 V.)

I0(L): Output Leakage Current (Data out is disabled, $0V \leq V_{out} \leq V_{cc}$)

VOH: Output High Voltage Level (IOH = -5.0mA)

VOL: Output Low Voltage Level (IOL = 4.2mA)

* NOTE: ICC1, ICC3, ICC4 and ICC6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. ICC is specified as an average current. In ICC1 and ICC3, address can be changed maximum two times while $\overline{RAS} = V_{IL}$. In ICC4, address can be changed maximum once within one page mode cycle.



CAPACITANCE (Ta = 25 °C, f=1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance [A0-A10]	CIN1	-	64	pF
Input capacitance [\bar{w}]	CIN2	-	70	pF
Input capacitance [$\overline{RAS0} - \overline{RAS2}$]	CIN3	-	42	pF
Input capacitance [$\overline{CAS0} - \overline{CAS3}$]	CIN4	-	30	pF
Input/Output capacitance [DQ0-31]	CDQ1	-	17	pF

AC CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, Vcc=5.0V ±10%. See notes 1,2.)

STANDARD OPERATION	Symbol	-50		-60		-70		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		ns	
Access time from \overline{RAS}	tRAC		50		60		70	ns	3,4
Access time from \overline{CAS}	tCAC		13		15		20	ns	3,4,5
Access time from column address	tAA		25		30		35	ns	3,11
\overline{CAS} to output in Low-Z	tCLZ	0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	13	0	15	0	20	ns	7
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	2
\overline{RAS} precharge time	tRP	30		40		50		ns	
\overline{RAS} pulse width	tRAS	50	10K	60	10K	70	10K	ns	
\overline{RAS} hold time	tRSH	13		15		20		ns	
\overline{CAS} hold time	tCSH	50		60		70		ns	
\overline{CAS} pulse width	tCAS	13	10K	15	10K	20	10K	ns	
\overline{RAS} to \overline{CAS} delay time	tRCD	20	37	20	45	20	50	ns	4
\overline{RAS} to column address delay time	tRAD	15	25	15	30	15	35	ns	11
\overline{CAS} to \overline{RAS} precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		10		15		ns	
Column address hold referenced to \overline{RAS}	tAR	40		45		55		ns	6
Column address to \overline{RAS} lead time	tRAL	25		30		35		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to \overline{CAS}	tRCH	0		0		0		ns	9
Read command hold time referenced to \overline{RAS}	tRRH	0		0		0		ns	9
Write command hold time	tWCH	10		10		15		ns	
Write command hold time referenced to \overline{RAS}	tWCR	40		45		55		ns	6
Write command pulse width	tWP	10		10		15		ns	
Write command to \overline{RAS} lead time	tRWL	15		15		20		ns	
Write command to \overline{CAS} lead time	tCWL	13		15		20		ns	



AC CHARACTERISITICS (continued)

STANDARD OPERATION	Symbol	-50		-60		-70		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Data-in set-up time	t _{DS}	0		0		0		ns	10
Data-in hold time	t _{DH}	10		10		15		ns	10
Data-in hold time referenced to $\overline{\text{RAS}}$	t _{DHR}	40		45		55		ns	6
Refresh period (2K Ref)	t _{REF}		32		32		32	ms	
Write command set-up time	t _{WCS}	0		0		0		ns	8
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ - before - $\overline{\text{RAS}}$ refresh)	t _{CSR}	10		10		10		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ - before - $\overline{\text{RAS}}$ refresh)	t _{CHR}	10		10		15		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	t _{RPC}	5		5		5		ns	
Access time from $\overline{\text{CAS}}$ precharge	t _{CPA}		30		35		40	ns	3
Fast Page mode cycle time	t _{PC}	35		40		45		ns	
$\overline{\text{CAS}}$ precharge time (Fast Page cycle)	t _{CP}	10		10		10		ns	
$\overline{\text{RAS}}$ pulse width (Fast Page cycle)	t _{RASP}	50	200K	60	200K	70	200K	ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ precharge time ($\overline{\text{C}}$ -B- $\overline{\text{R}}$ refresh)	t _{WRP}	10		10		10		ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ hold time ($\overline{\text{C}}$ -B- $\overline{\text{R}}$ refresh)	t _{WRH}	10		10		10		ns	
$\overline{\text{CAS}}$ precharge time ($\overline{\text{C}}$ -B- $\overline{\text{R}}$ cycle)	t _{CPT}	20		20		30		ns	



NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles before proper device operation is achieved.
2. VIH (min) and VIL (max) are reference levels for measuring timing of input signals. Transition times are measured between VIH (min) and VIL (max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2TTL loads and 100pF.
4. Operation within the tRCD (max) limit insures that tRAC (max) can be met. tRCD (max) is specified as a reference point only. If tRCD is greater than the specified tRCD (max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD \geq tRCD (max).
6. tAR, tWCR, tDHR are referenced to tRAD (max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
8. tWCS is non-restrictive operating parameter. It is included in the data sheet as electrical characteristic only. If tWCS \geq tWCS (min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
9. Either tRCH or tRRH must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles.
11. Operation within the tRAD (max) limit insures that tRAC (max) can be met. tRAD (max) is specified as a reference point only. If tRAD is greater than the specified tRAD (max) limit, then access time is controlled by tAA.



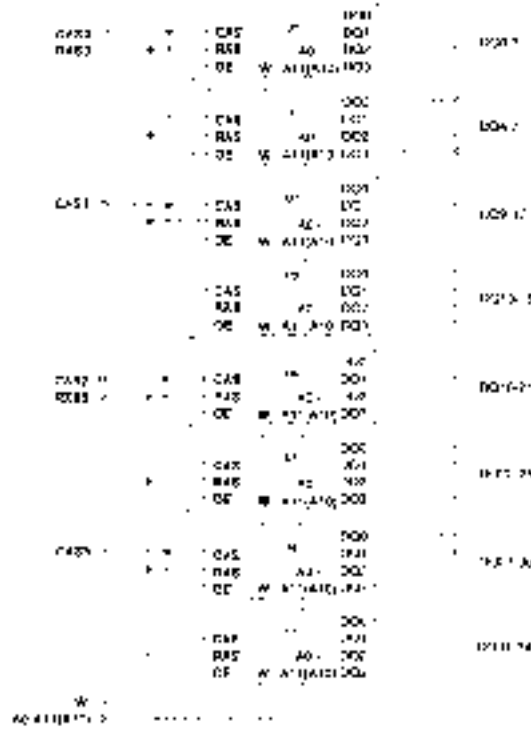
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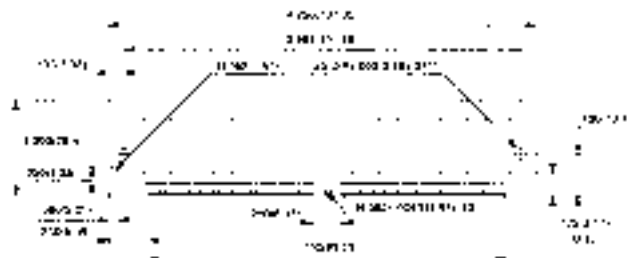
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FUNCTIONAL BLOCK DIAGRAM



PACKAGE DIMENSIONS



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